Hafnia-based ferroelectric tunnel junctions

Bhagwati Prasad, Vishal Thakare, Alan Kalitsov, Zimeng Zhang, and Ramamoorthy Ramesh

Tunneling electroresistance effect

Ferroelectric tunnel junctions (FTJs)

Brief history:

1970: Polar switch concept proposed by Esaki *et. al*.

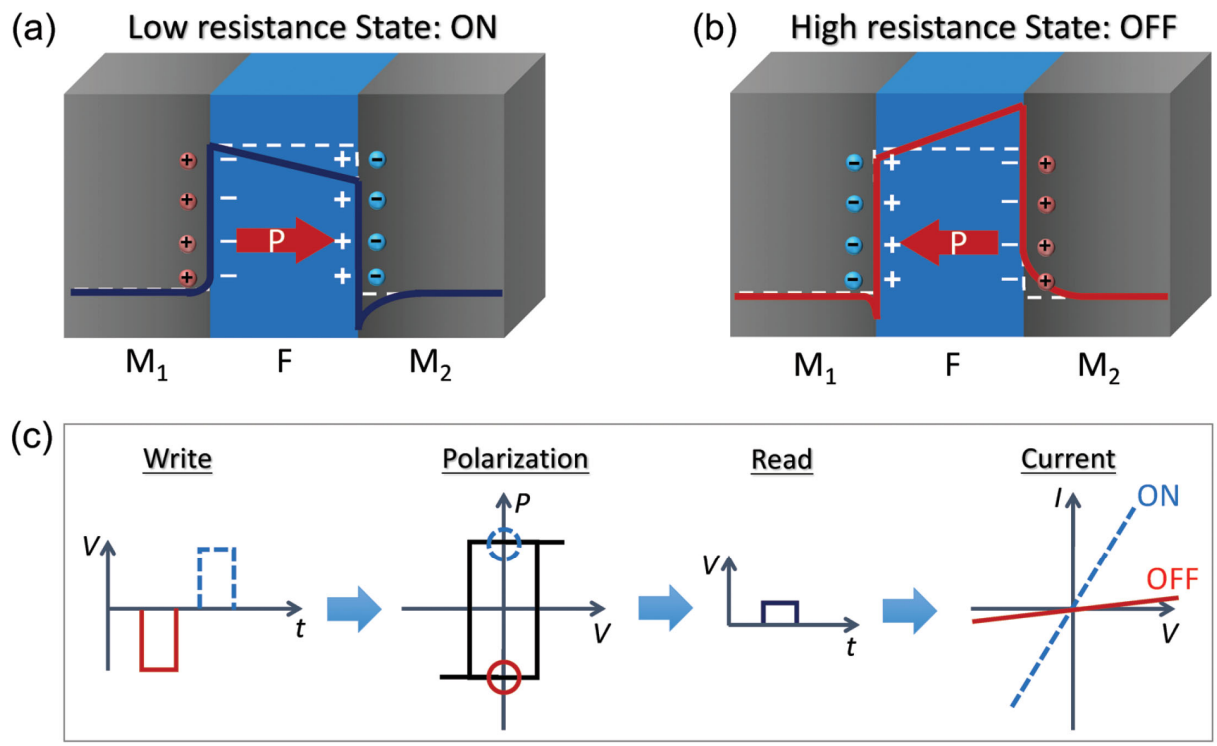
2003: Ferroelectricity in ultrathin films was demonstrated

2009: TER effect in BTO-based junctions (*Nature* and *Science* papers) was observed

Why FTJ is important?

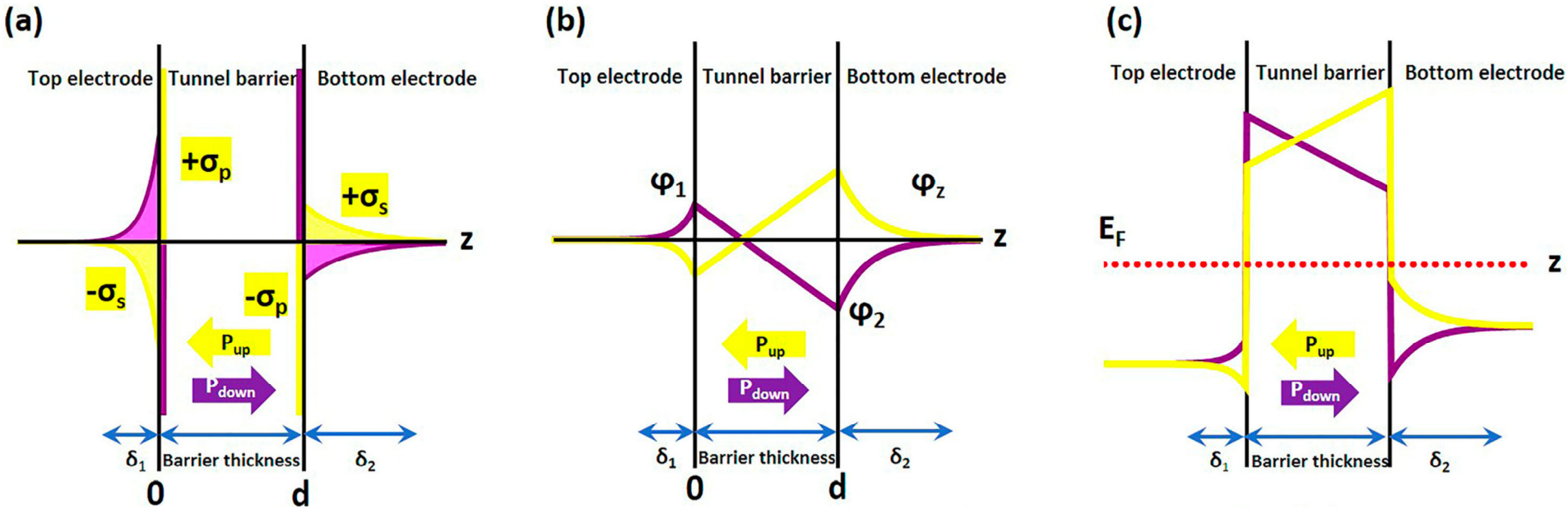
- High (ns) speed write/read
- Low power consumption ~ fJ/bit
- Nondestructive readout (unlike FeRAMs)
- High-density data storage : crossbar-type memory arrays?

OFF/ON ratio : 100 (FTJ) vs 4 (MRAM)



i. Asymmetrical deformation of the barrier potential profile
ii. Changes in the density of states at the barrier/electrode interfaces
iii. Voltage-dependent variation of the barrier thickness due to piezoelectricity

Tunneling electro resistance effect: Potential Profile Across the barrier



Charge distribution

Electrostatic potential profile

Band diagram

Ref: Applied Physics Reviews **7**, 011304 (2020)

$\delta_1 < \delta_2$

ON/OFF ratios of various FTJ devices explored in last 10 years

ON/OFF ratio = J_{ON}/J_{OFF}

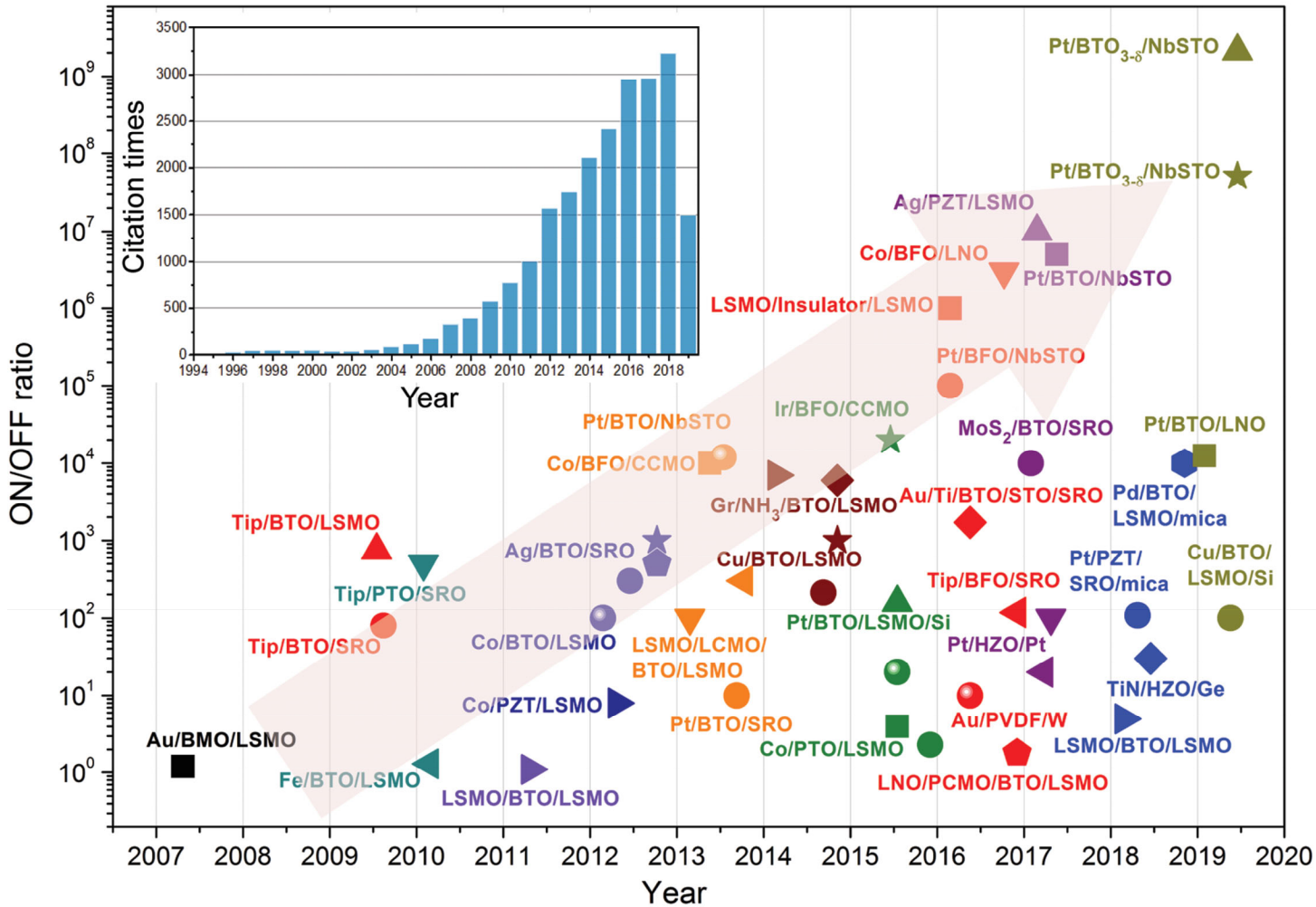
$$TER = \frac{J_{ON} - J_{OFF}}{J_{OFF}} X\ 100\ \%$$

Ferroelectric tunnel junctions:
MFM tunnel junctions

Bottom electrodes: $SrRuO_3$ (SRO), $La_{0.67}Sr_{0.33}MnO_3$ (LSMO), $LaNiO_3$ (LNO),and $Ca_{0.96}Ce_{0.04}MnO_3$ (CCMO) to achieve the epitaxial growth of ferroelectric barriers

Top Electrodes: Metals, such as Pt, Au, Fe, and Co

Typically metal have smaller screening lengths than the oxide



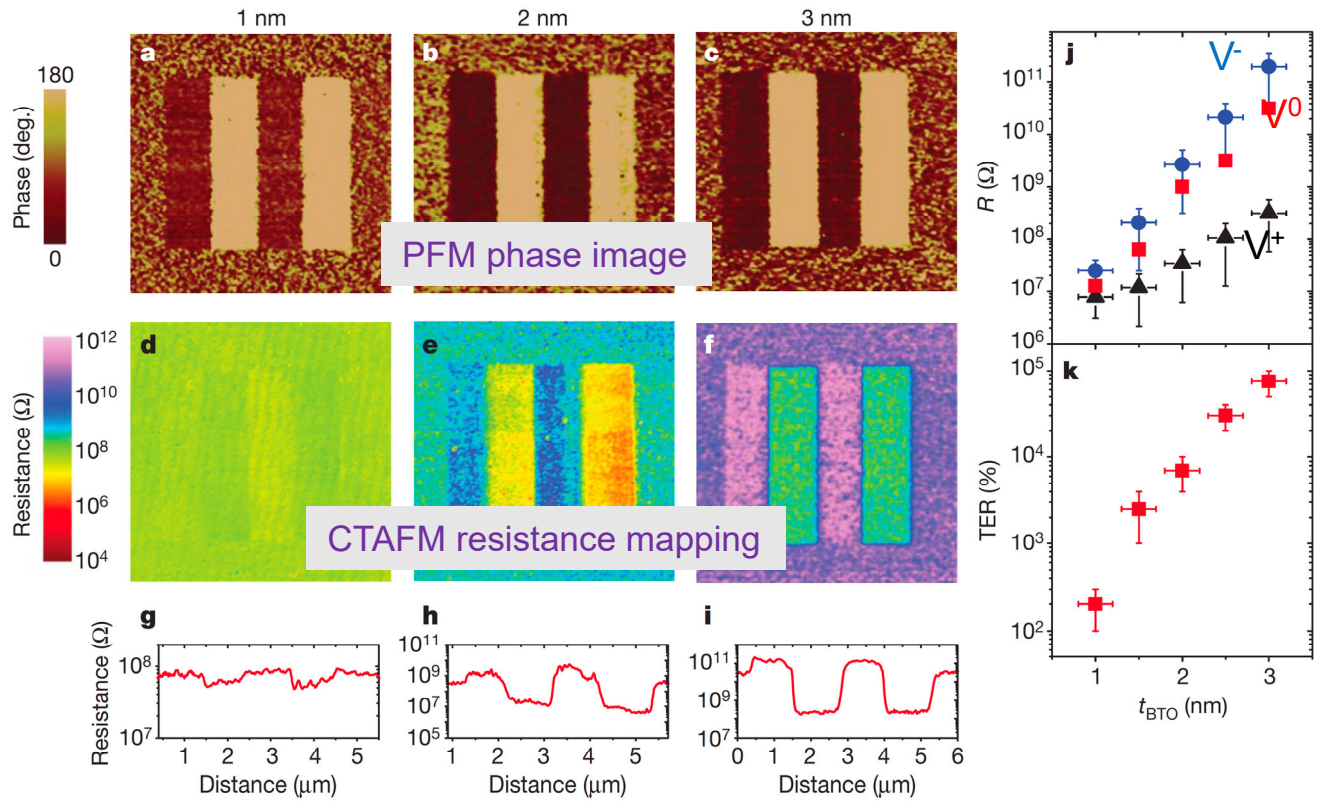
Adv. Mater. **2019**, 1904123

Early experiments

- Demonstrated highly strained BTO films retain robust room-temperature ferroelectricity down to 1 nm
- Used conductive-tip atomic force microscopy
- Electroresistance effect scales exponentially with ferroelectric film thickness, reaching 75,000% at 3 nm
- Demonstrated scalability down to 70 nm

Giant tunnel electroresistance for non-destructive readout of ferroelectric states

V. Garcia[1,2], S. Fusil[1,3], K. Bouzehouane[1], S. Enouz-Vedrenne[4], N. D. Mathur[2], A. Barthélémy[1] & M. Bibes[1]



V_{write} ~ ± 3.5 V

Conductive-tip/BTO (1,2 and 3nm)/LSMO(30 nm)/NGO (001) substrate

Vol 460|2 July 2009|doi:10.1038/nature08128 (2009) nature

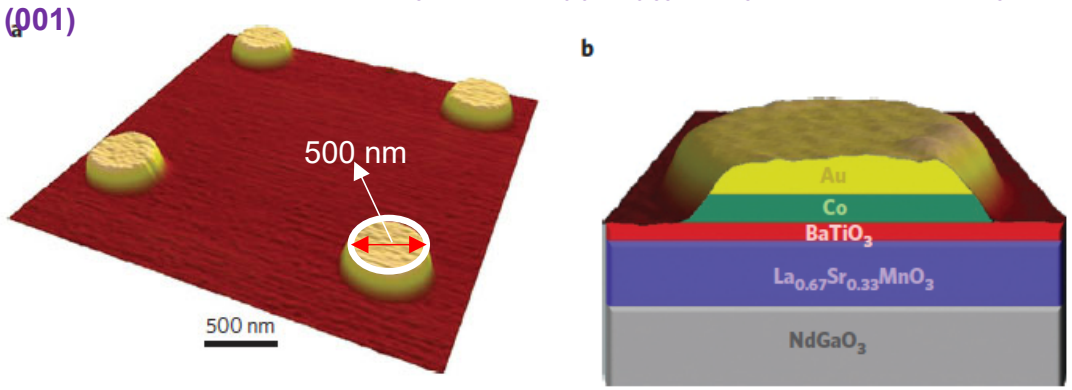
Early experiments

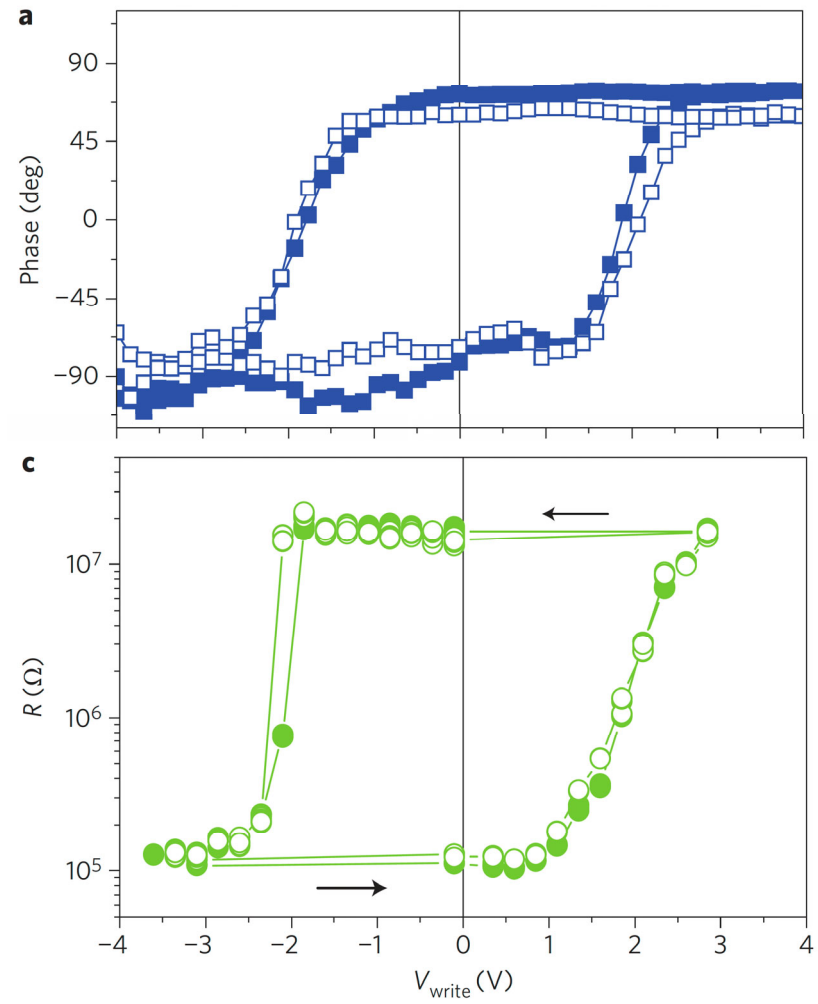
nature nanotechnology (2012) LETTERS
PUBLISHED ONLINE: 4 DECEMBER 2011 | DOI: 10.1038/NNANO.2011.213

Solid-state memories based on ferroelectric tunnel junctions

André Chanthbouala[1], Arnaud Crassous[1], Vincent Garcia[1]*, Karim Bouzehouane[1], Stéphane Fusil[1,2], Xavier Moya[3], Julie Allibe[1], Bruno Dlubak[1], Julie Grollier[1], Stéphane Xavier[4], Cyrile Deranlot[1], Amir Moshar[5], Roger Proksch[5], Neil D. Mathur[3], Manuel Bibes[1] and Agnès Barthélémy[1]

Au(10 nm)/Co(10 nm)/$BaTiO_3$(2 nm)/$La_{0.67}Sr_{0.33}MnO_3$(30 nm)// $NdGaO_3$ (001)

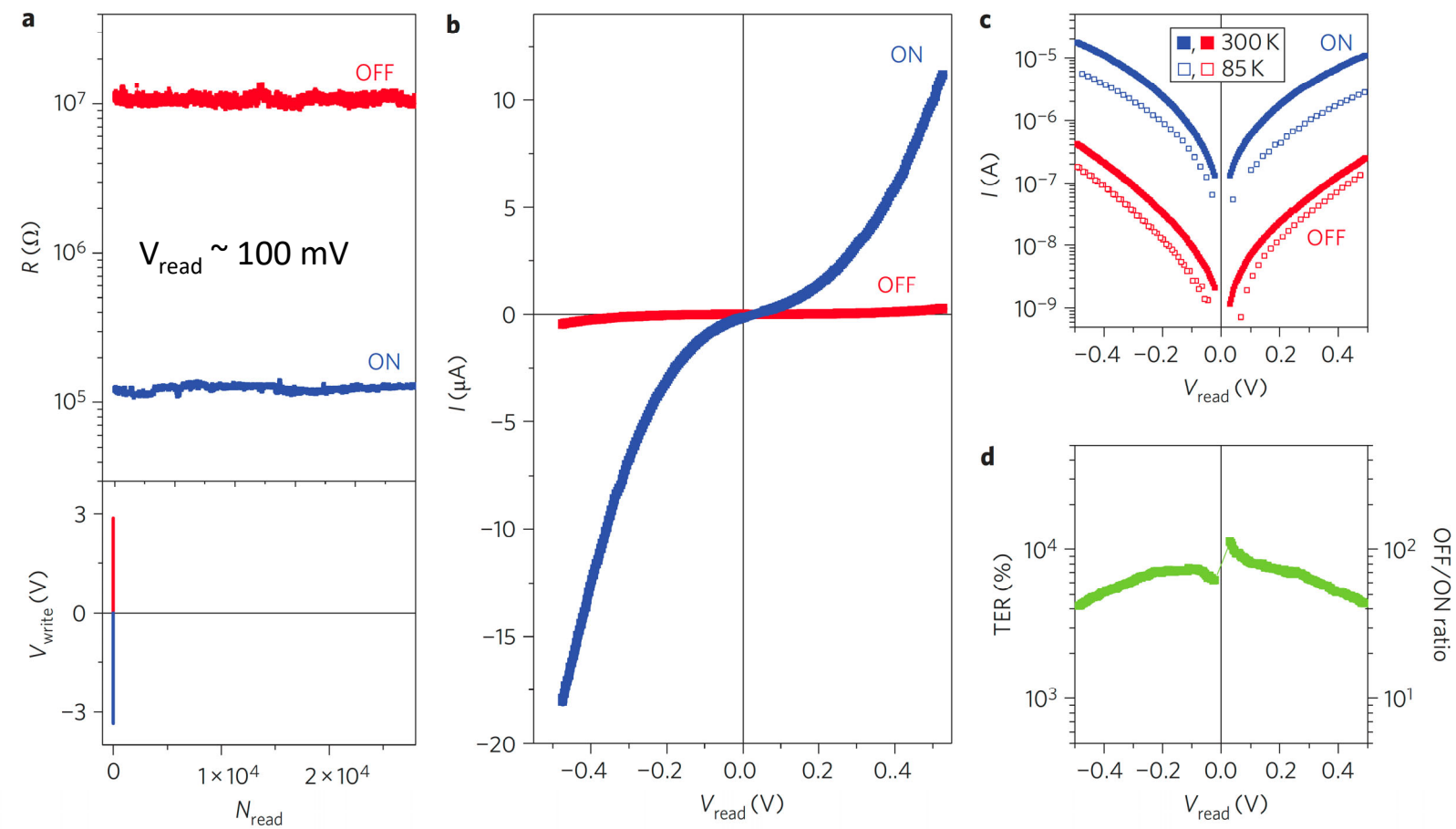




AFM conducting tip used

Voltage pulse (V_{write}) = 100 µs
V_{read} = 100 mV << V_C

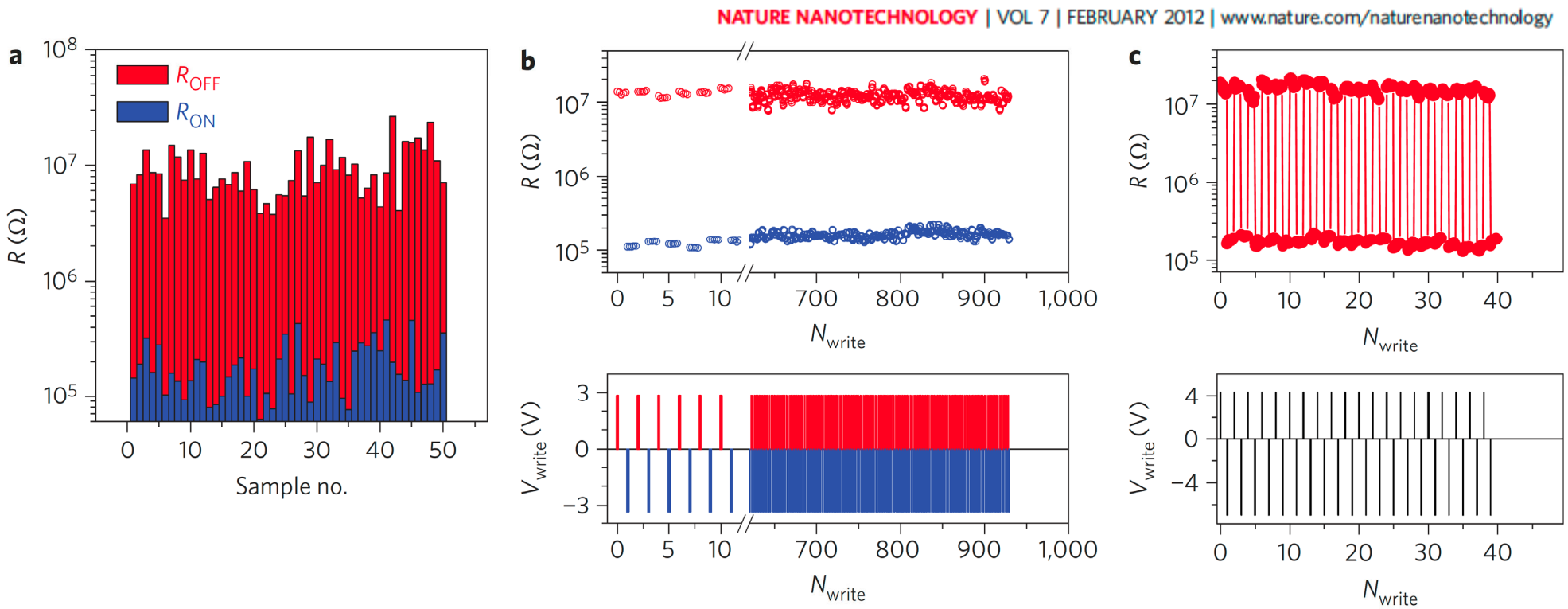
Early experiments: Read



- TER effect of ~ 10,000% with OFF/ON ratio ~100
- I (V_{read}) shows tunneling behavior

NATURE NANOTECHNOLOGY | VOL 7 | FEBRUARY 2012 | www.nature.com/naturenanotechnology

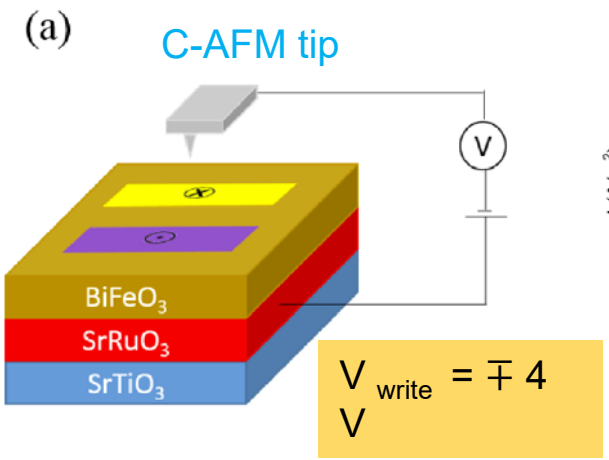
Early experiments: Write

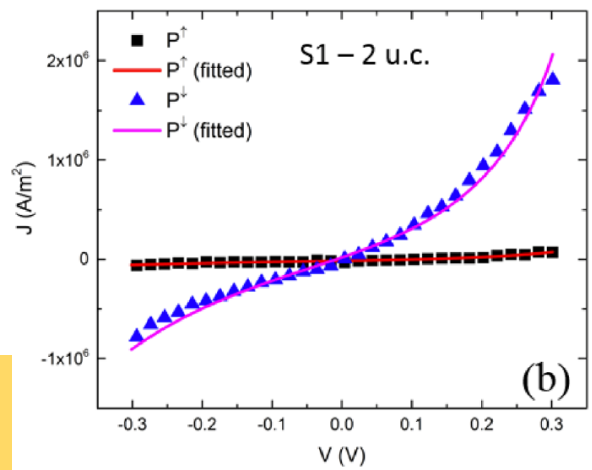


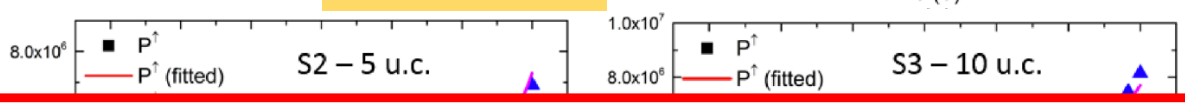
10 ns pulse

- Average OFF/ON ratio of 64 (50 junctions) : High yield and good uniformity
- Fatigue tests : 900 write/read cycles (Voltage pulse (V_{write}) = 100 µs)
- High (> 100 OFF/ON) ratio has been achieved with the write voltage pulse of 10ns
- Calculated energy ~ 10-100 fJ/bit
- Demonstrated device performance with 50 nm wide nanojunctions

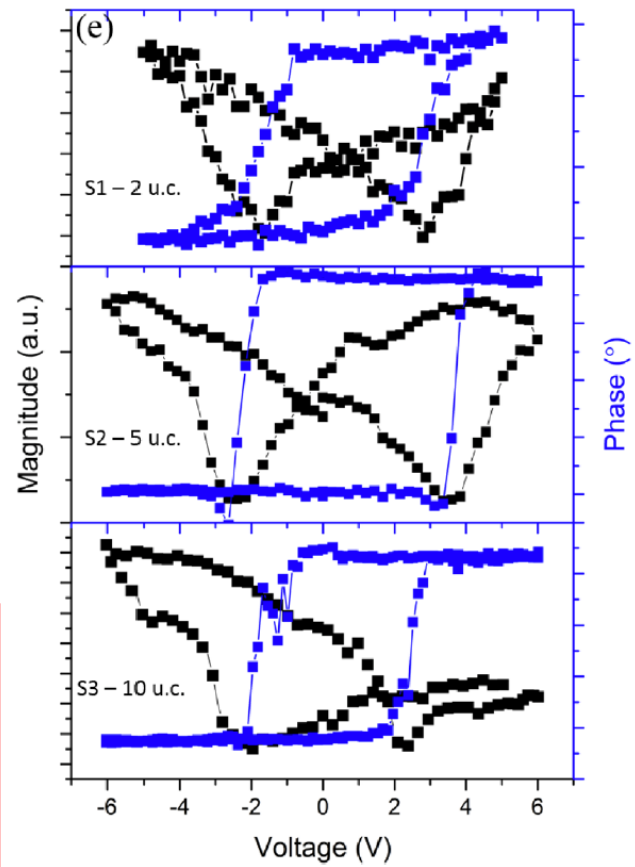
Ultrathin ferroelectric barrier layer







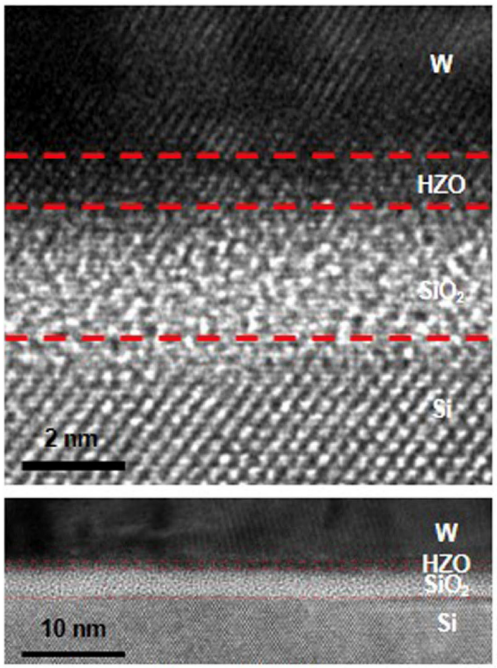
Sample	Thickness (u.c.)	$\Delta\varphi$ (eV)	TER ratio (%) ($V_{read} = +0.3$ V)
S1	2	0.26	2700
S2	5	0.55	11800
S3	10	0.63	9700



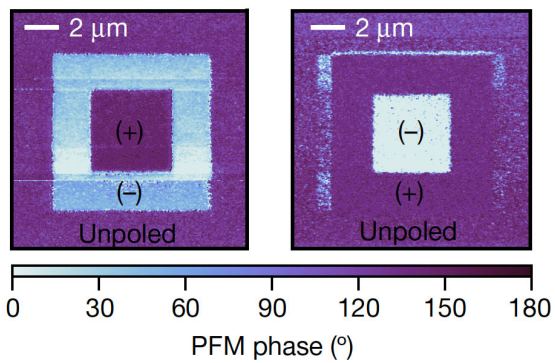
PFM phase and amplitude hysteresis loops

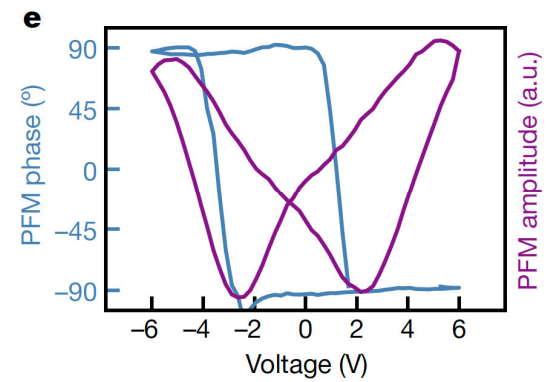
Appl. Phys. Lett. 109, 242901 (2016)

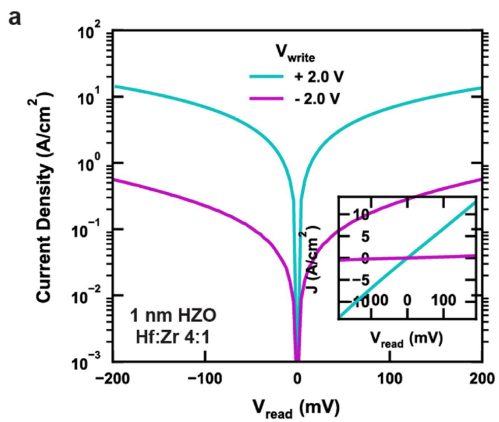
Enhanced ferroelectricity in ultrathin films grown directly on silicon

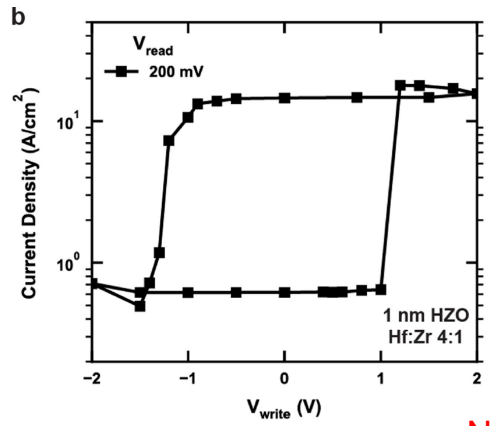


10 cycles HZO







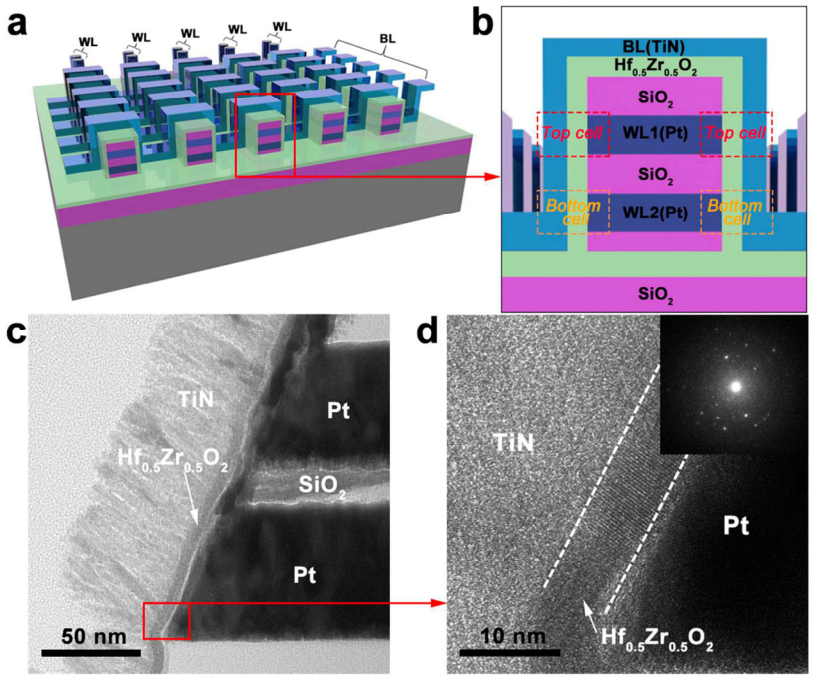


Nature 482, 580 (2020)

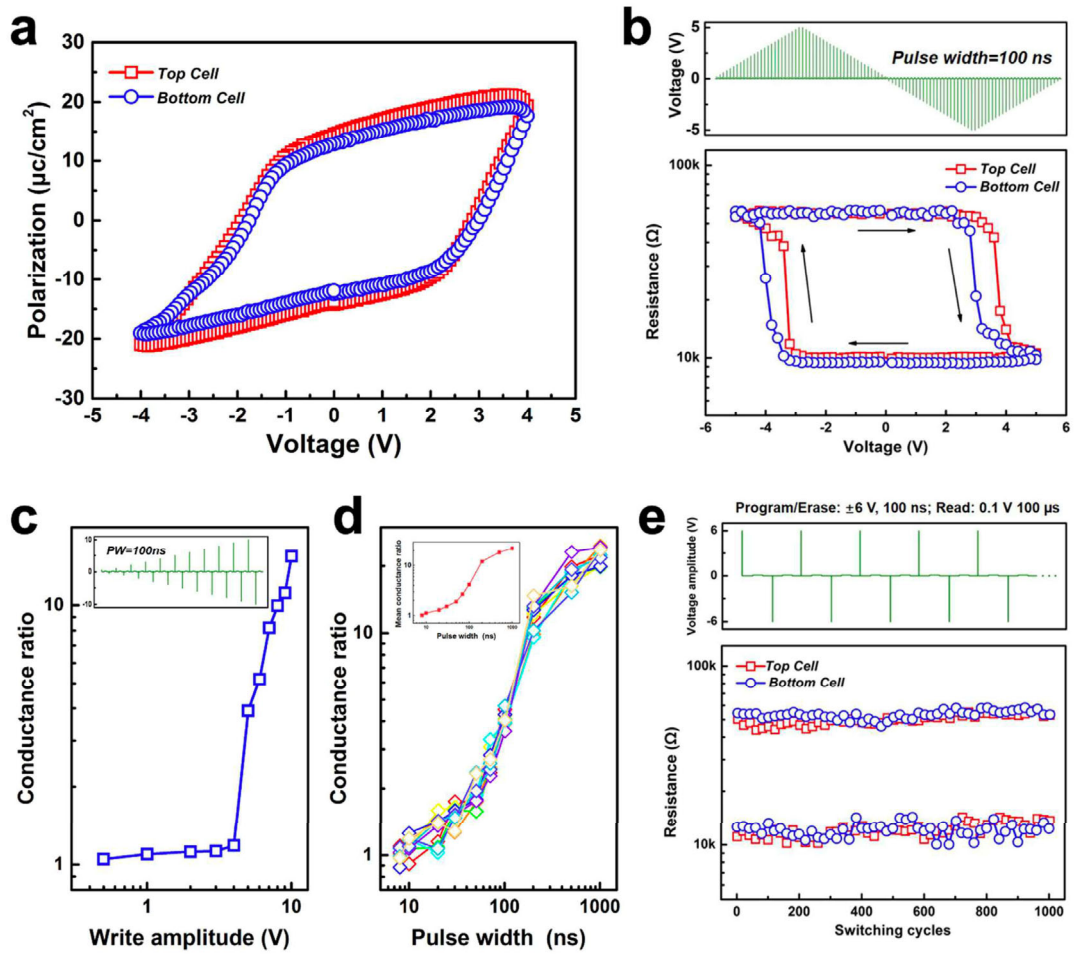
- Thin films of HZO were grown by ALD
- After ALD deposition, a top metal (W or TiN) is deposited by sputtering at room temperature
- A rapid post-metal annealing at 500 °C stabilizes the desired polar orthorhombic phase

3D vertical ferroelectric HZO-based FTJ array

Ultra-low Power $Hf_{0.5}Zr_{0.5}O_2$ based Ferroelectric Tunnel Junction



Nanoscale, 2018



- HZO barrier layer was deposited by ALD technique
- Write voltage : ± 6V for 100 ns

Device performance with different FTJs

Structure	OFF/ON	Switching speed	Endurance
Pt/Co/BFO/CCMO	$>10^4$	$\sim$0.1 μs	$>10^3$ cycles
Co/Au/BTO/LSMO	$\sim$300	10 ns	Not specified
Pt/Co/BFO/CCMO	$>10^4$	Not specified	$>$2000 cycles
Pt/BFO/NSTO	$\sim10^3$	Not specified	Not specified
Co/PZT/LSMO	$>$100	$\sim$0.1 μs	Not specified
Pr or Ag/PZT/Pt	$\sim10^6$	$\sim$5 μs	$>$100 cycles
Pd/HZO/LSMO	$\sim$160	Not specified	$\sim10^6$ cycles
TaN/HZO/Pt	$\sim$5	Not specified	$>10^3$ cycles
LSMO/BTO/LSMO	$>$5	6 ns	Not specified
Au/P(VDF-TrFE)/NSTO	$\sim10^4$	20 ns	Not specified
Co/BTO/LSMO	$>10^4$	$<$10 ns	Not specified
Pt/BTO/NSTO	$\sim10^5$	Not specified	Not specified
Au/Co/BTO/LSMO	$\sim10^3$	Not specified	Not specified
Pt/BTO/NSTO	$\sim10^6$	$\sim$10 ns	$>10^5$ cycles
Pt/$Sm_{0.1}Bi_{0.9}FeO_3$/NSTO	$\sim10^5$	$\sim$10 ns	$\sim10^6$ cycles
Best system	**10^5-10^6**	**< 10 ns**	**10^5-10^6 (Write + read)**

Device performance: MRAM vs FTJ

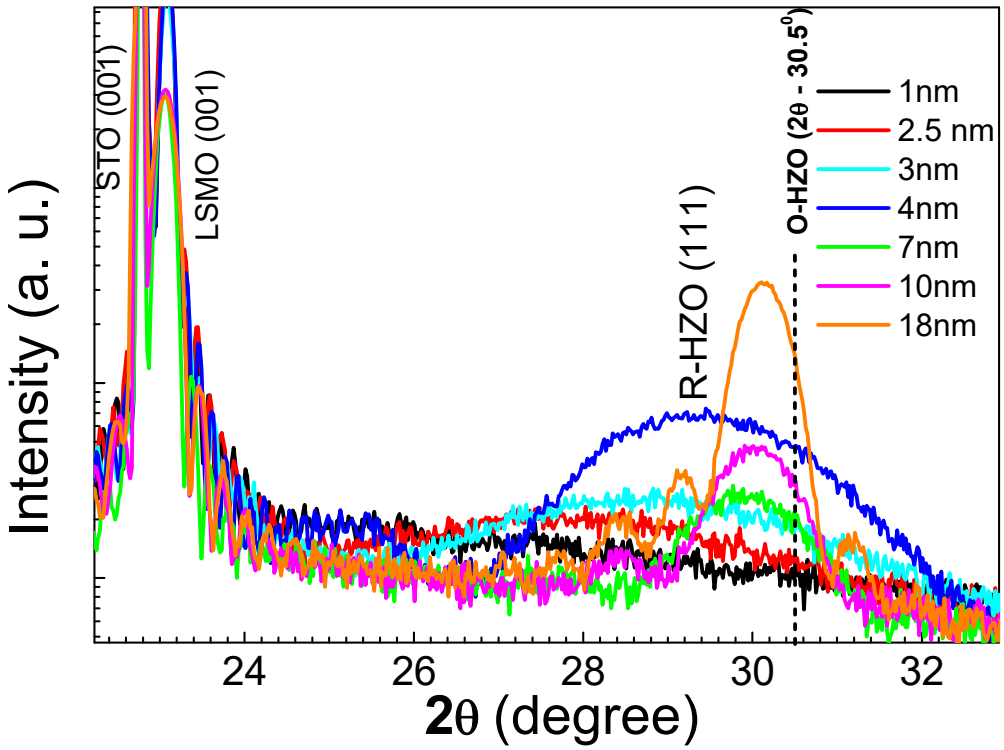
Specs	MRAM (For single device) 15+ Years of maturity (University Research and Industrial R&D)	FTJ (Best data) Nascent (University Research)
Smallest device size	20 nm	30-100 nm
V_w	0.5-1V	0.3-2 V
V_R	0.3-0.5 V	0.1-0.3 V
Pulse	10-50 ns	10-50 ns
Endurance	10^8 cycles	10^6 cycles
Retention	~10 Years	~ 10 Years
OFF/ON	3	100+
Write Power (J)	pJ/bit	fJ/bit
RA (1 nm barrier)	~10 $\Omega\mu m^2$	$k\Omega\mu m^2$

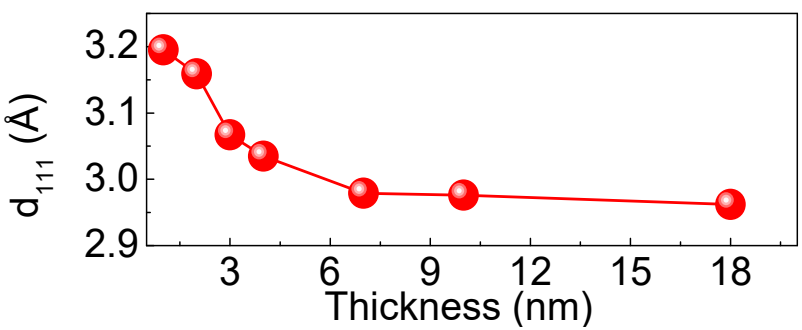
Can we integrate FTJ structure with CMOS devices?

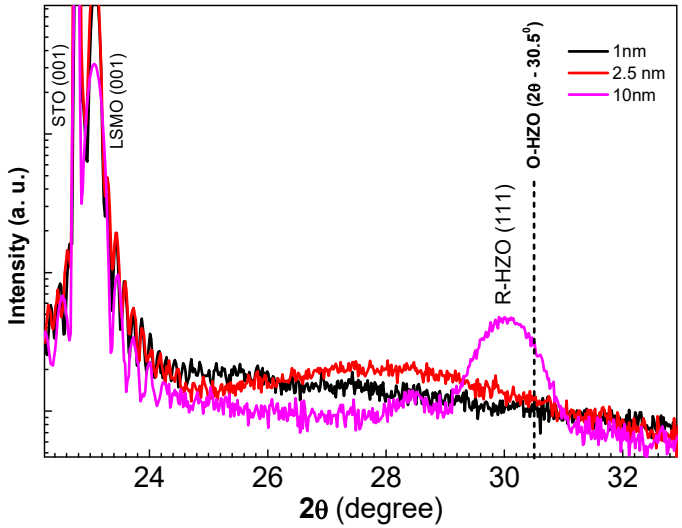
Why Hafnia is better candidate than Perovskite for FTJ-based memory technology?

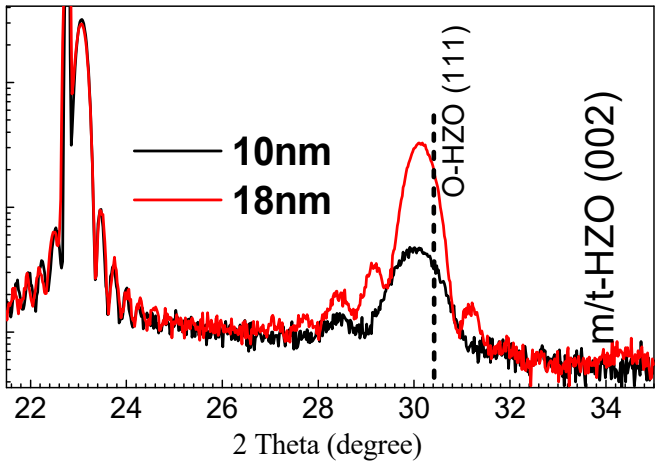
- **Growth** : ALD (no special electrode and epitaxy requirement)
- **Si-Integration**: known since1990 as a High-k dielectric
- **Ferroelectricity** : 1-30 nm thick films (stress state, doping, grain size, etc.)
- **Scaling** : Can follow CMOS
- **3D integration**: Due to ALD process and known knowledge
- **Ferroelectric coercive field:** 10 X of perovskite
- Ferroelectric polarization ~ Similar to perovskite

XRD patterns of HZO/LSMO (60 nm)//STO (001) samples









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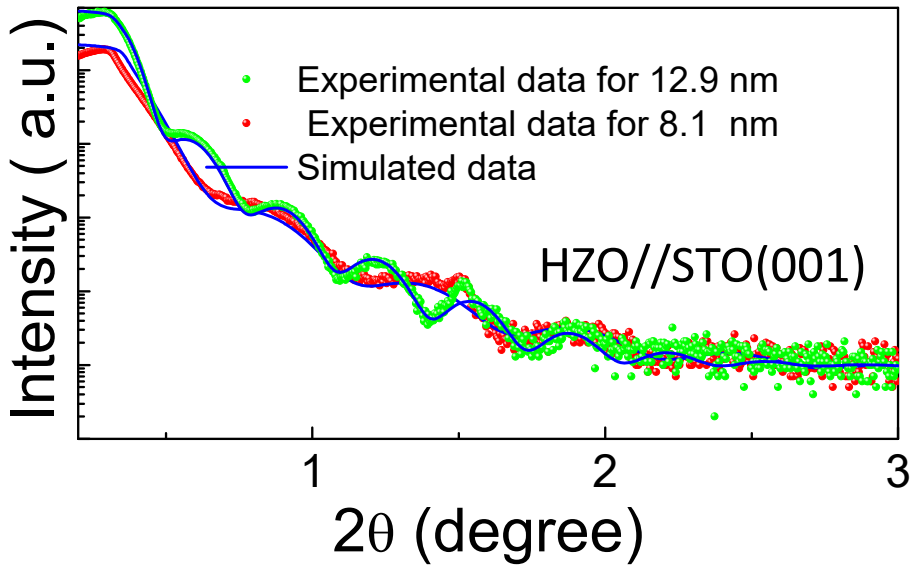
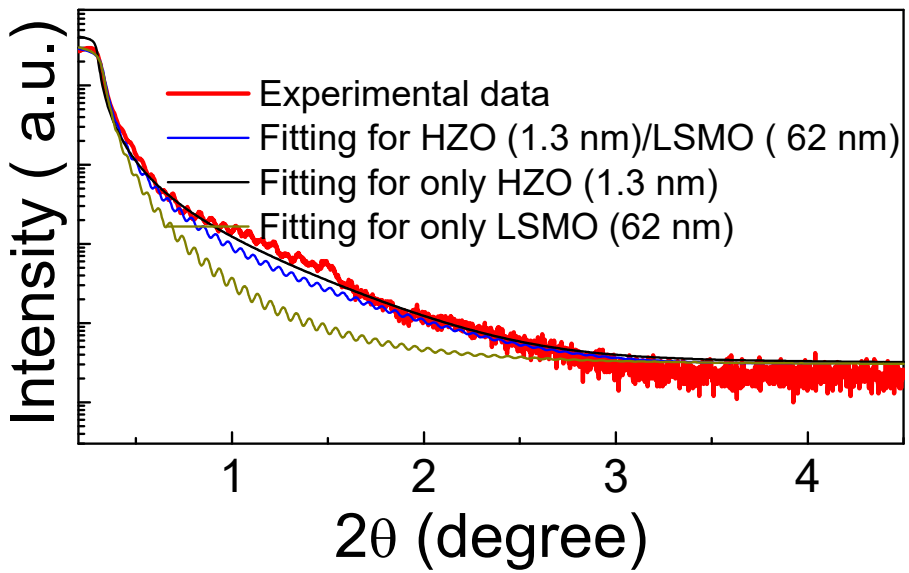
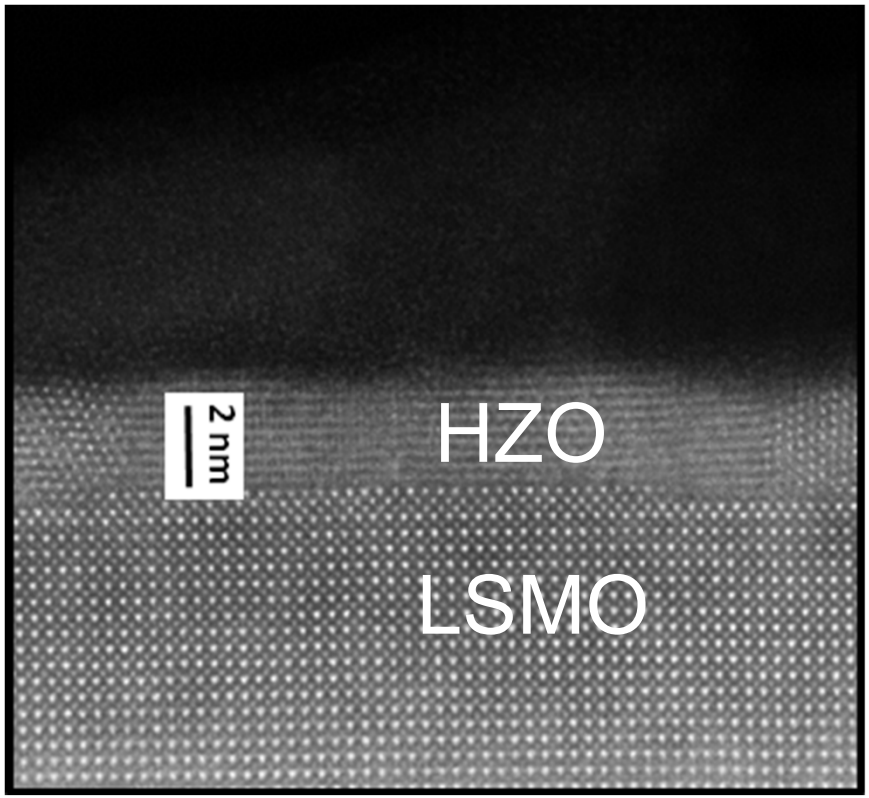
- The in-plane compressive strain increases with reducing film thickness below 10 nm
- Additional peak around 34.5° for 18 nm thin film indicates the appearance of the monoclinic phase

XRR and HRTEM of HZO/LSMO (60 nm)//STO (001) samples







HRTEM

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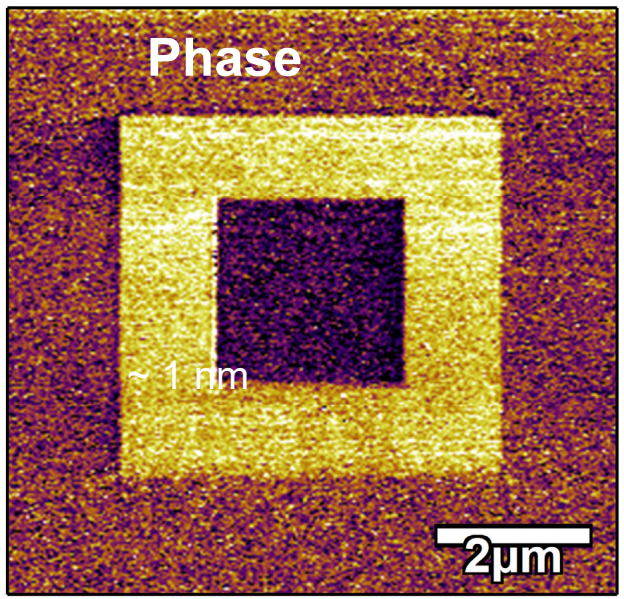
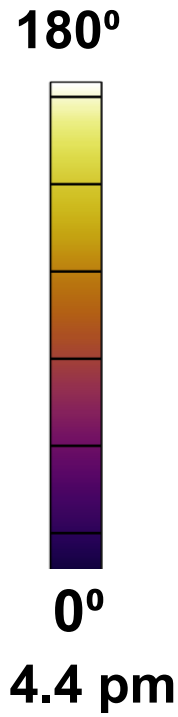
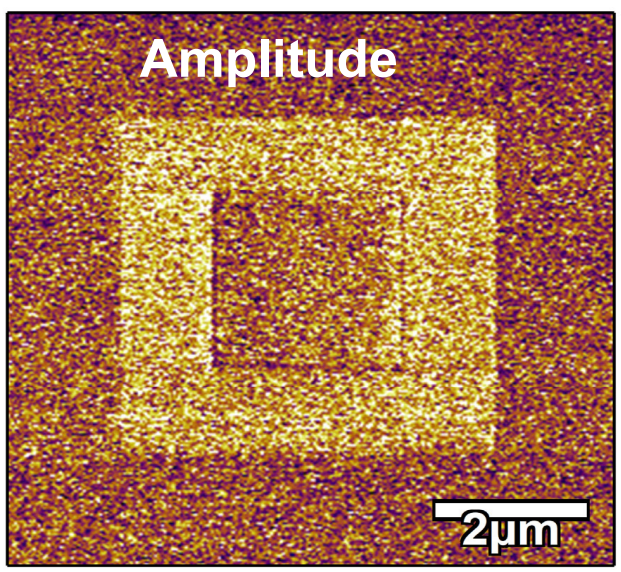
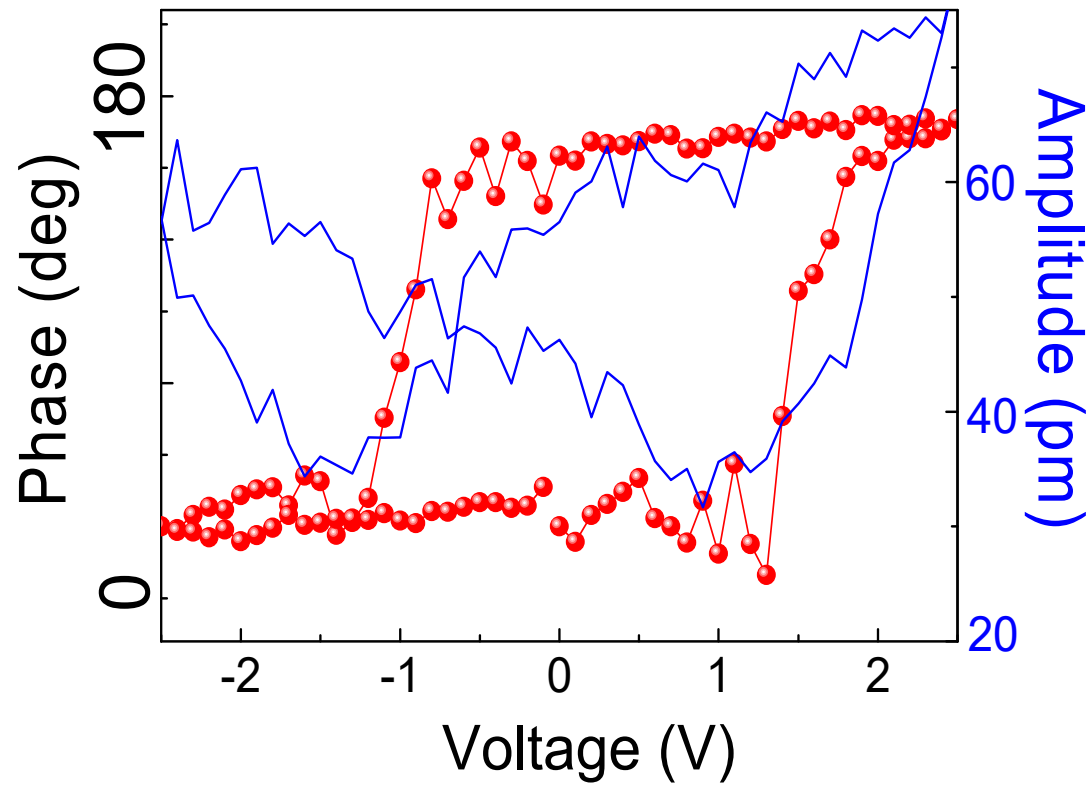
PFM imaging of HZO (1 nm)/LSMO (60 nm)//STO (001) samples





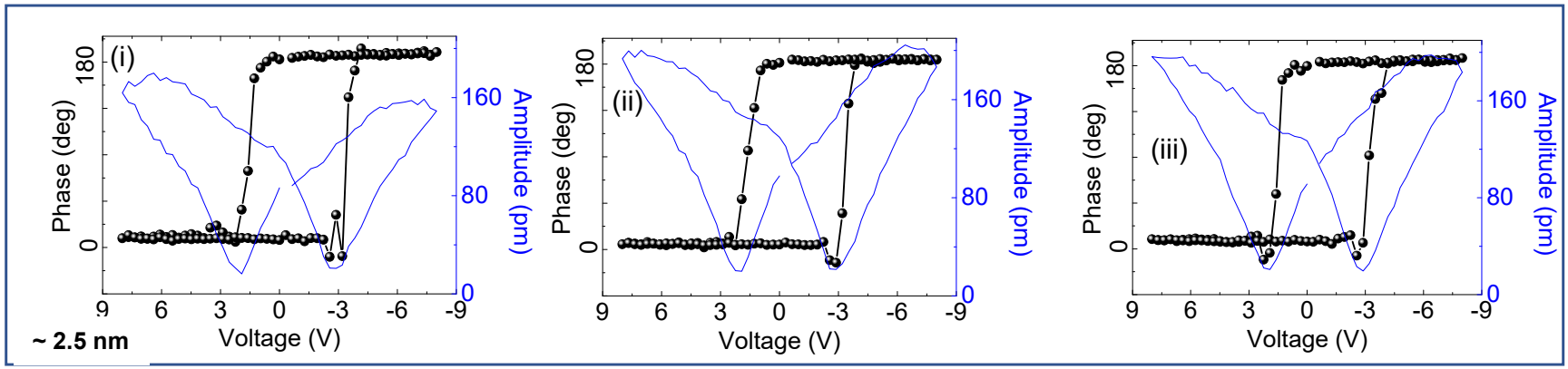


Phase (red) and amplitude (blue) signal of the local hysteresis loop

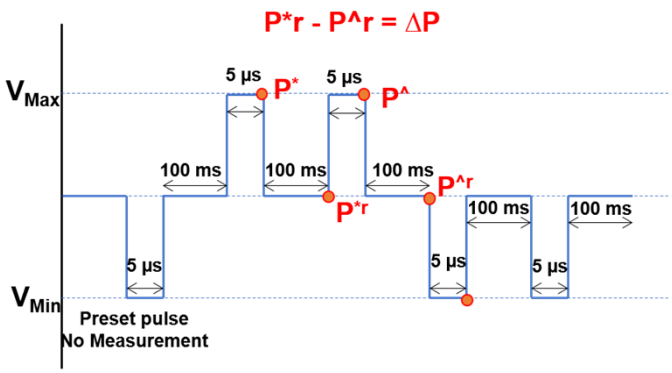


- Phase contrast image shows bistable remanent polarization states
- The signal at the domain walls in amplitude contrast image is almost zero, which suggests the charging effects are low

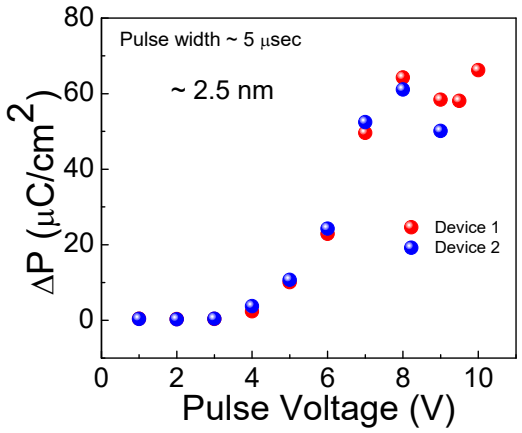
Ferroelectric property of HZO/LSMO (60 nm)//STO (001) samples



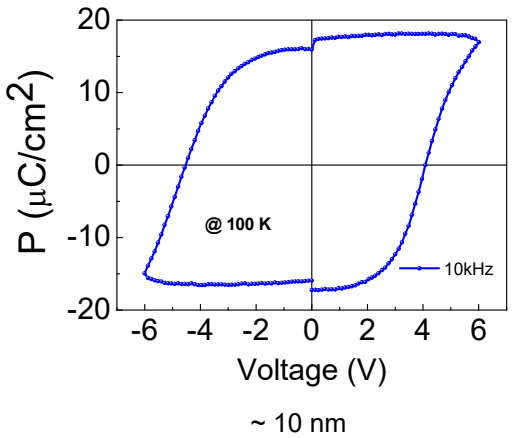
The local PFM phase and amplitude hysteresis loops, acquired at the three different places on the ~2.5 nm HZO films



Schematics of the voltage pulse for PUND measurement



PUND characterization of ~ 2.5 nm HZO film, showing the remanent polarization of ~ 30 µC/cm2



Ferroelectric hysteresis loop at 10 kHz of a 10 nm HZO film

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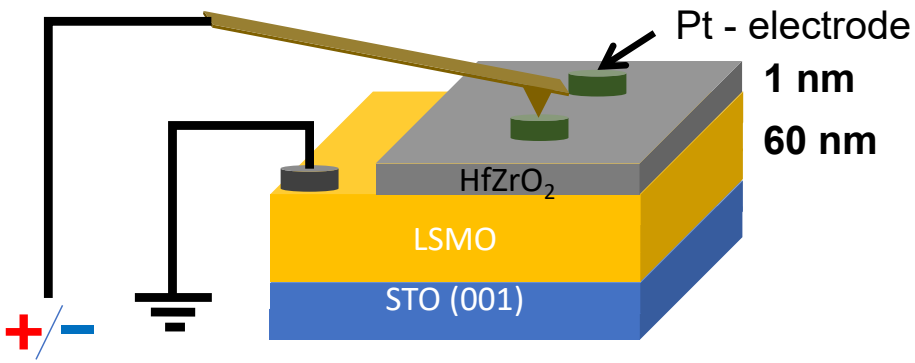
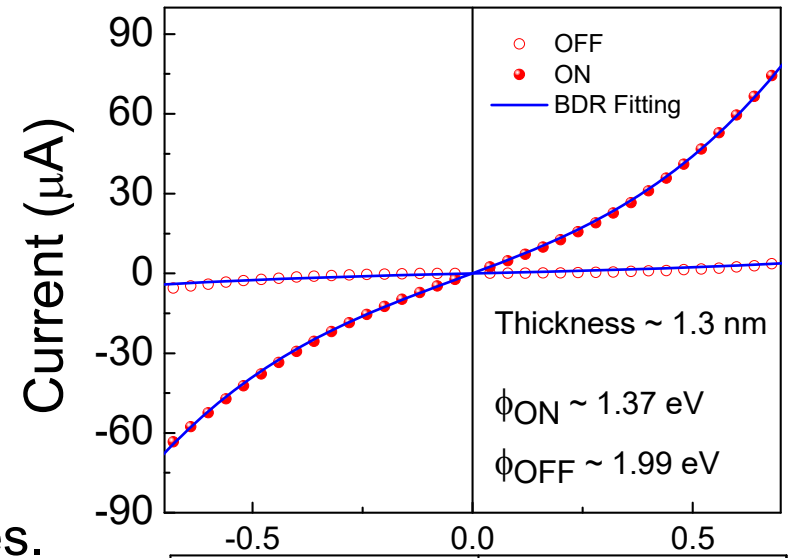
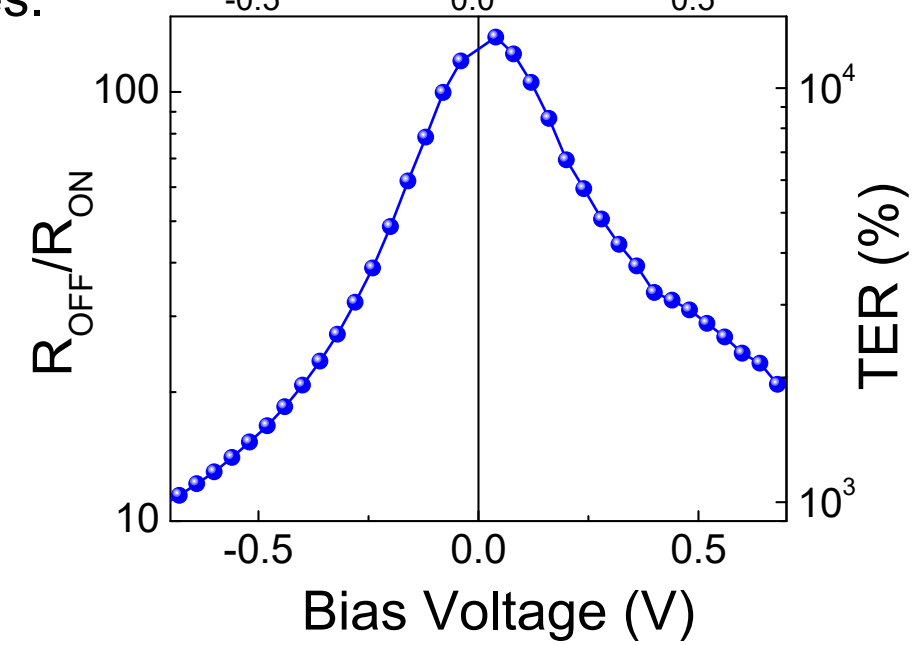
TER effect in Pt/HZO(1 nm)/LSMO FTJ devices



Schematic of ultrathin HZO tunnel devices.



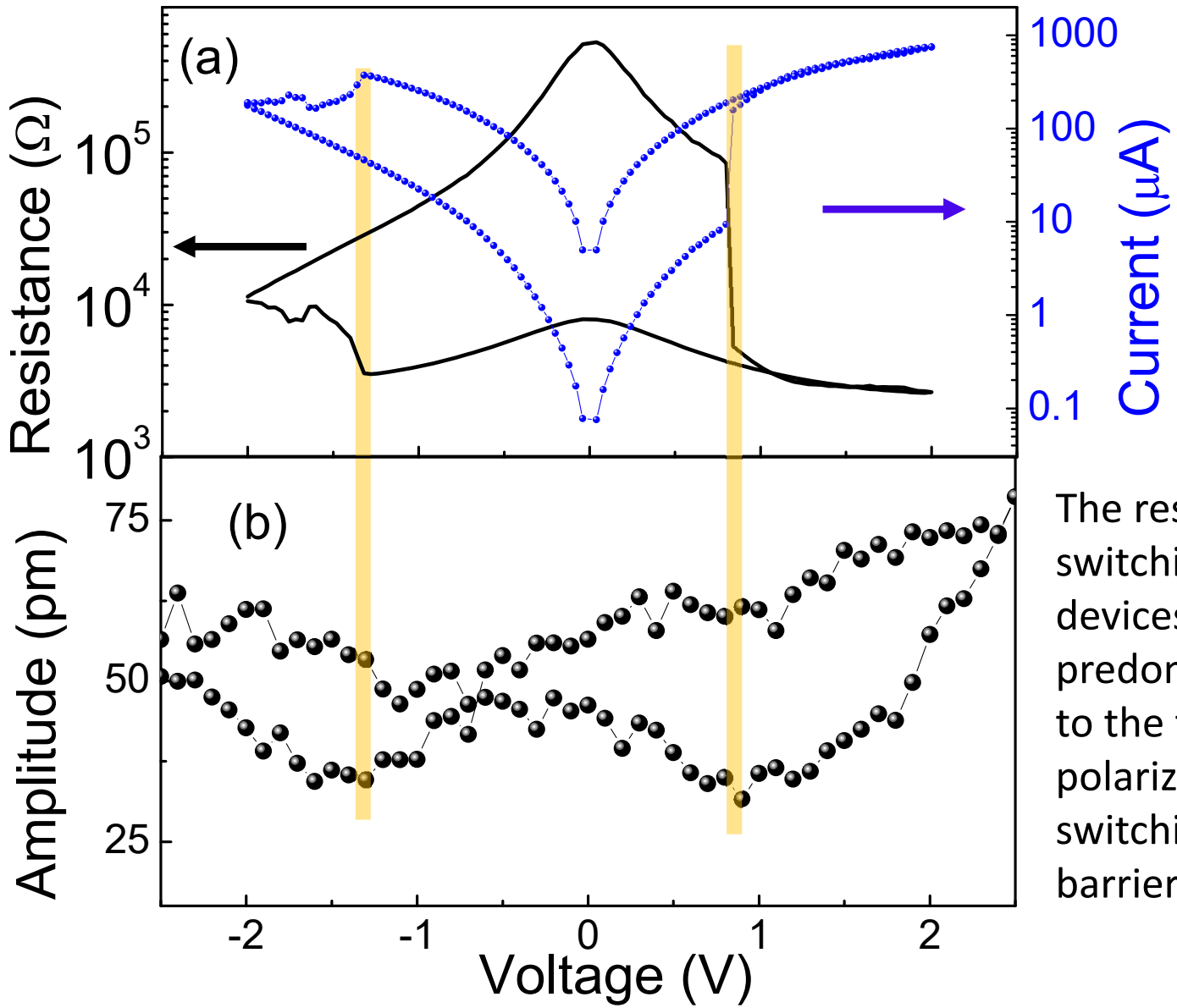


- I–V data fitted with BDR tunneling model
- OFF/ON junction resistance ratio of 135 was achieved at zero bias
- ON-state RA product of ≈25 kΩμm^2 at 300 mV

TER effect in Pt/HZO(1 nm)/LSMO FTJ devices

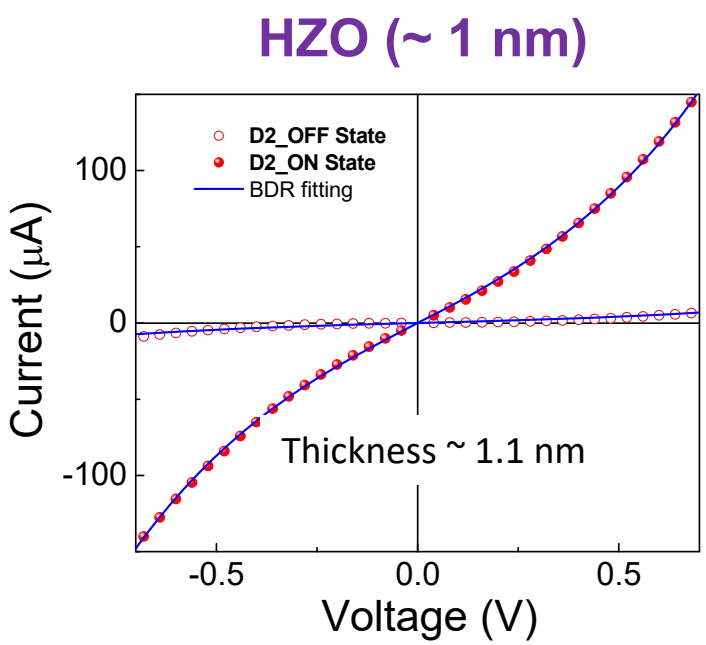
Junction resistance (Current) versus write voltage pulse

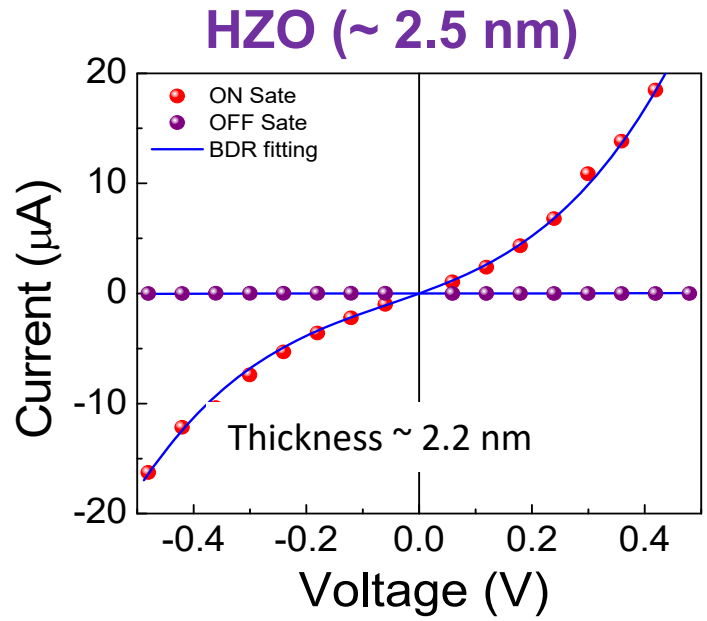
PFM amplitude hysteresis loop

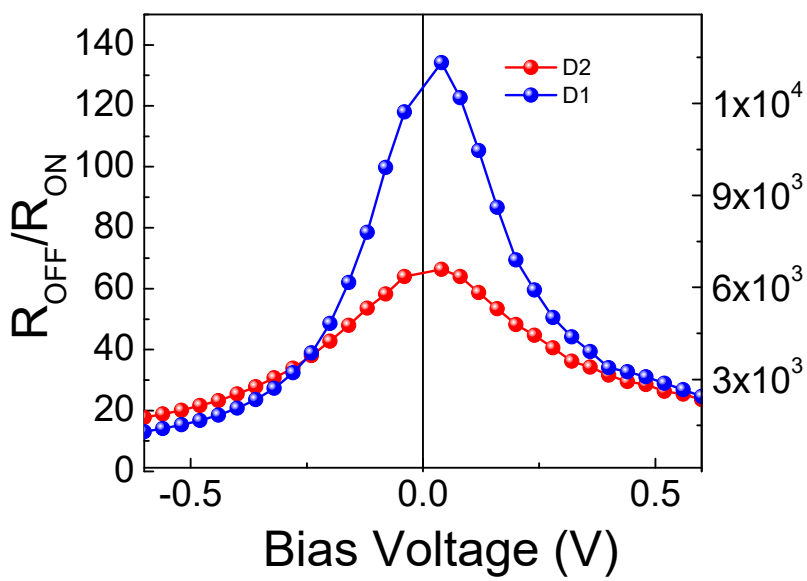


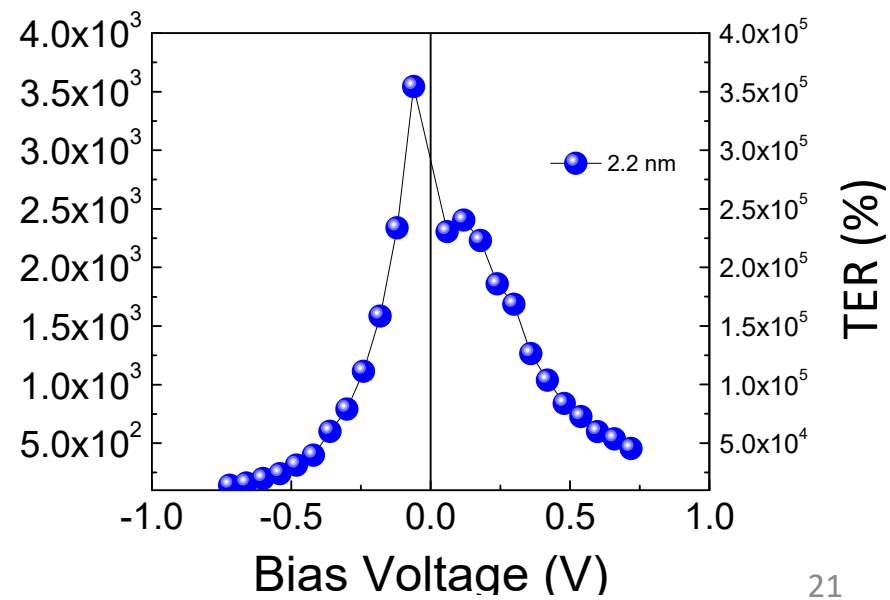
The resistance switching in FTJ devices is predominantly due to the ferroelectric polarization switching of the barrier layer

TER effect in Pt/HZO/LSMO FTJ devices









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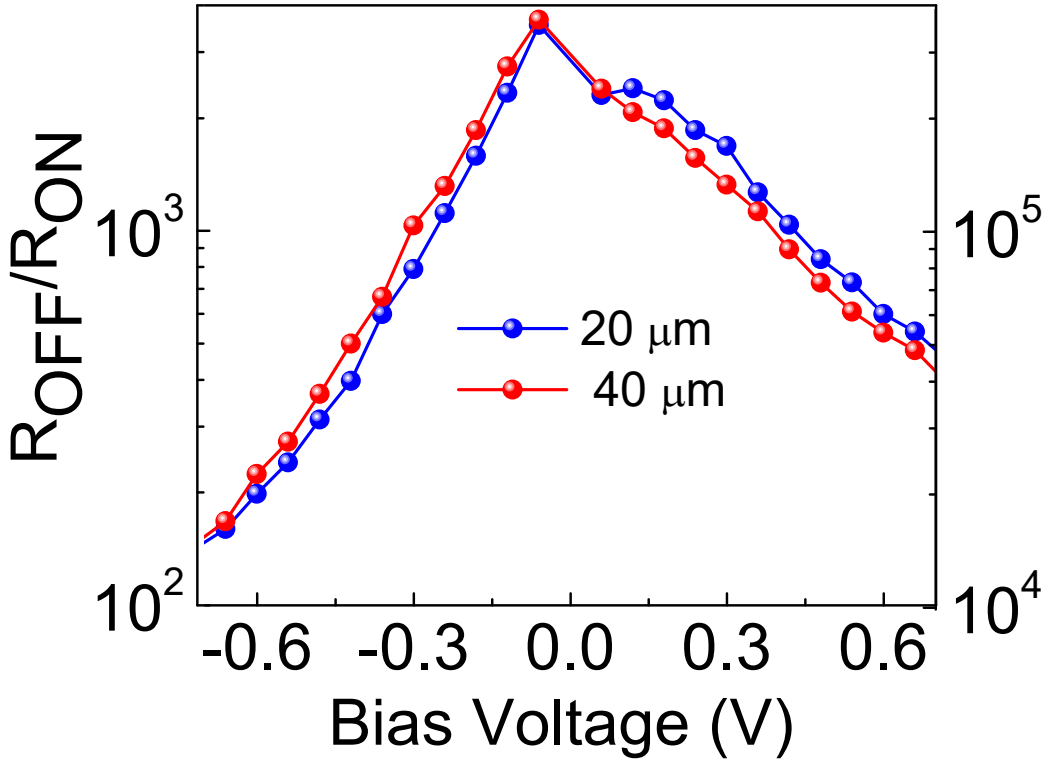
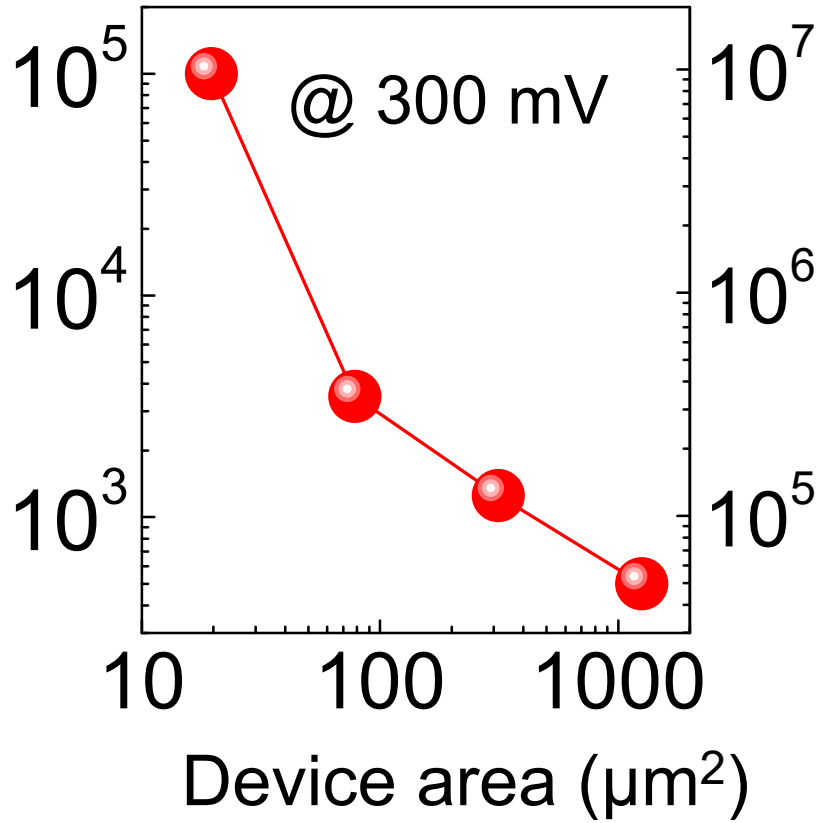
TER effect in Pt/HZO/LSMO FTJ devices: Does device size matter?





TER ratio ≈10^7% @300 mV with the device area of 25 μm²

OFF/ON ratio (TER%) of the tunnel devices with ≈2.5 nm tunnel barrier as a function of the junction area

Summary

- FTJ devices investigated within the last 10 years have shown promising properties as non-volatile resistive memory element, including large OFF/ON ratios, reproducibility, high speed (ns-ps) and potentially low operation energy (fJ/bit)
- **Why doped HfO_2?:** Scalability (3D integration), Si-integration compatibility, robust ferroelectricity in ultrathin films and known knowledge of ALD growth
- Robust ferroelectricity is achieved with ≈1 nm films by stabilizing the rhombohedral polar phase of HZO (R-HZO) through a large compressive strain
- The OFF/ON ratio of the junction resistance at zero bias is about 135 with ≈1 nm thick barrier, which increases to ≈10^5 with increasing the barrier thickness to ≈2.5 nm
- The resistance-area product (RA) of tunnel junctions is reduced by nearly three orders of magnitude
- These results set the stage for further exploration of Hafnia-based FTJs for non-volatile memory applications