



# Checking Robustness to Weak Persistency Models

Hamed Gorjiara University of California, Irvine Weiyu Luo University of California, Irvine Alex Lee University of California, Irvine

Harry Xu University of California, Los Angeles Brian Demsky University of California, Irvine

• Non-volatile, byte-addressable, and highspeed





• Non-volatile, byte-addressable, and highspeed

- Challenge:
  - The program needs to guarantee crash-consistency



load store





PMEM DIMM

Supporting crash consistency

• Ordering: existence of processor cache









Supporting crash consistency

• Ordering: existence of processor cache











Supporting crash consistency

• Ordering: existence of processor cache











Supporting crash consistency

• Ordering: existence of processor cache









Supporting crash consistency

- Ordering: existence of processor cache
- Durability: using cache instructions



In x86:

clwb

sfence





#### State-of-the-Art

- Constructive approaches
- Testing and checking frameworks

## State-of-the-Art

- Constructive approaches
- Testing and checking frameworks

- + Systematically transforming programs
- Only on lock-free data structure
- Inject unnecessary flush and fence<sup>[2,3,4]</sup>
- Memory overhead<sup>[1]</sup>

Mirror: Friedman et. al. PLDI'2021
 Izraelevitz et. al. DISC'2016
 Dananjaya et. al. ASPLOS'20
 Venkataraman et. al. FAST'11

## State-of-the-Art

- Constructive approaches
- Testing and checking frameworks

- Bugs with visible symptoms<sup>[5,6]</sup>
- User annotation or heuristics<sup>[1-4]</sup>
- Manual inspection of long execution trace<sup>[1-6]</sup>

1]	Witcher
2j	PMTest
3]	PMDebugger
4]	XFDetector

[5] Jaaru [6] Yat

## **Strict Persistency**

- A persistency model where
  - Persistency memory order = Volatile Memory order



## **Strict Persistency**

- A persistency model where
  - Persistency memory order = Volatile Memory order
- Naïve implementation
  - Using flush instructions after each memory operation



## **Key Observation**

Typical correct use of flush instructions in PM programs ensures:

Program executions under weak persistency semantics are equivalent to those under strict persistency semantics



#### Timeline

#### Weak Persistency Models



#### Timeline

Weak Persistency Models



#### Timeline

#### **Identical Post-crash Execution**

#### Robustness



#### Timeline

Weak Persistency Models



#### Timeline

#### **Reads-from Relation**

#### Robustness



#### Timeline

**Weak Persistency Models** 



#### Timeline

#### Sequenced-before Relation

#### Robustness



#### Timeline

Weak Persistency Models



#### Timeline



#### Timeline

Weak Persistency Models

#### **TSO Ordering**



#### Timeline

A program is **robust** to a weak persistency model:

• For **any** crash event and **any** post-crash execution under the weak persistency model, there **exists** some execution under strict persistency model that is equivalent to it.

A program is **robust** to a weak persistency model:

• For **any** crash event and **any** post-crash execution under the weak persistency model, there **exists** some execution under strict persistency model that is equivalent to it.

Robustness is sufficient condition to assure correct usage of flush and fence operations

#### **Robustness and Commit Store**



## **Our Solution: PSan**

Persistent Memory Sanitizer (PSan):

- Dynamically checks robustness for programs
- Detects bugs caused by missing flushes/fences
- Bug localization
- Suggests bug fixes

## **PSan Overview**

 Built on top of Jaaru



## **PSan Overview**

- Built on top of Jaaru
- Random vs. model checking mode



• PSan computes a set of strictly persistent executions whose precrash executions are consistent with the post-crash execution



- Reason about the potential crash interval
  - Using constraints







- Reason about the potential crash interval
  - Using constraints





Pre-crash Code	
1. x = 1 2. y = 2 3. x = 3 4. y = 4 5. x = 5	









- Each thread can make different progress when a program crashes
- Each thread requires its own potential crash interval constraints
- Deducing constraints
  - TSO ordering between stores to the same variable





Post-crash execution

Rx = 1



Pre-crash execution



Pre-crash execution



Pre-crash execution



Pre-crash execution



Pre-crash execution



- Each thread can make different progress when a program crashes
- Each thread requires its own potential crash interval constraints
- Deducing constraints
  - TSO ordering between stores to the same variable
  - Happens-before relation

Pre-crash execution



Pre-crash execution



Pre-crash execution



Pre-crash execution



• Defining a fix as a set of flush intervals

Two cases for robustness violations:

- 1. Reading from too old of store
- 2. Reading from too new of store

**Pre-crash execution** 

Post-crash execution





**Pre-crash execution** 

Post-crash execution





**Pre-crash execution** 

Post-crash execution



#### Reads from a store that is too old



**Pre-crash execution** 

Post-crash execution





**Pre-crash execution** 

Post-crash execution





Case 2: Reading from too new of store

**Pre-crash execution** 

Post-crash execution





Case 2: Reading from too new of store

**Pre-crash execution** 

Post-crash execution





Reads from a store that is too new Case 2: Reading from too new of store

**Pre-crash execution** 



Pre-crash execution

Post-crash execution



Special case: Multithreaded programs

Rx = 0

Ry = 1

Pre-crash execution

Post-crash execution



Special case: Multithreaded programs

Pre-crash execution

Post-crash execution



Flush interval is empty!!

Special case: Multithreaded programs

Pre-crash execution



Evaluated PSan on:

- A collection of data structure: RECIPE, CCEH, Fast Fair
- Popular real-world frameworks and applications: PMDK, Memcached, and Redis

PSan found 48 bugs of which 17 are new!

- Missing flush and fence operations
- Cache line alignment bugs
- Memory management bugs

- Missing flush and fence operations
- Cache line alignment bugs
- Memory management bugs

```
btree::btree(){
    root = (char*)new page();
    // clflush((char*)root, sizeof(page));
    height = 1;
    // clflush((char*)this, sizeof(btree), false, true);
}
```

- Missing flush and fence operations
- Cache line alignment bugs
- Memory management bugs

```
class header{
        page* leftmost_ptr;
        page* sibling_ptr;
        uint32_t level;
        uint32_t switch_counter;
        std::mutex *mtx;
        union Key highest;
        uint8_t is_deleted;
        int16_t last_index;
        uint8_t dummy[5];
};
```

- Missing flush and fence operations
- Cache line alignment bugs
- Memory management bugs
  - Garbage collection, memory allocation components

- Negligible overhead compared to Jaaru
- Average **13.1s** to explore all executions revealing all bugs for each benchmark



Jaaru vs. PSan

#### Conclusion

Testing persistent memory program is **challenging**, and fixing persistency bugs is **difficult**!

#### PSan

- Presents robustness, a sufficient correctness condition
- Finds persistency bugs caused by missing flushes/fences
- Found 48 persistency bugs of which 17 are new
- Localizes persistency bugs and suggests fixes
- Available on: plrg.ics.uci.edu/psan

