Ferroelectric, Analog Resistive Switching in BEOL Compatible TiN/$HfZrO_4$/TiO_x Junctions

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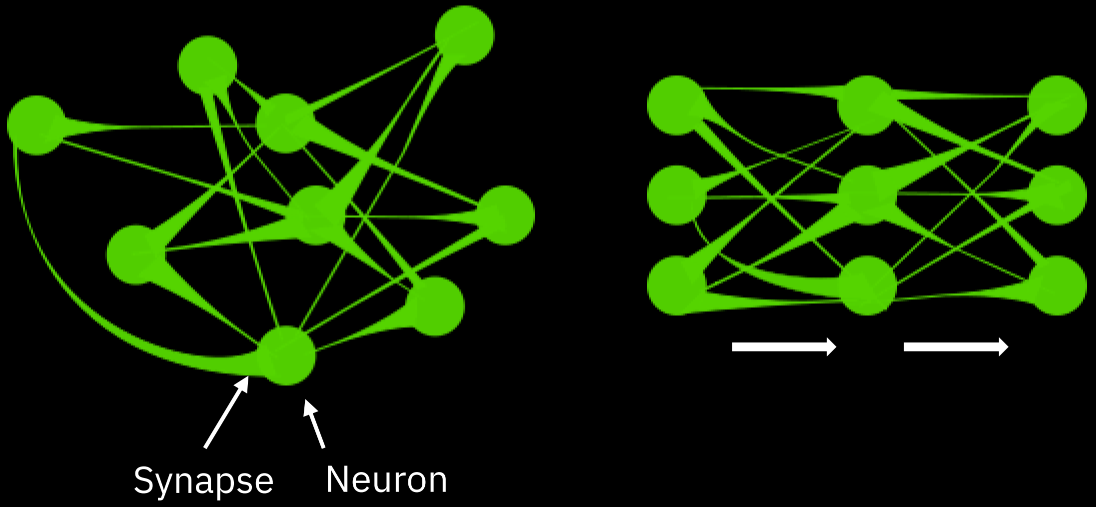
IBM

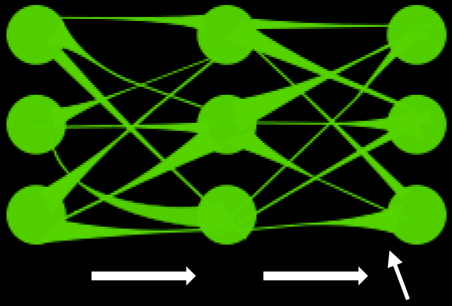
Motivation
Memristive ferroelectric junction
Results
Conclusion

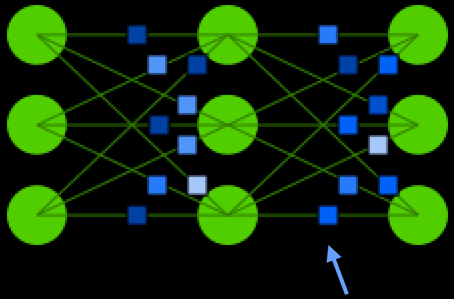
Mimicking the brain, "Deep-Learning" algorithms are structured into layers of interconnected neurons.



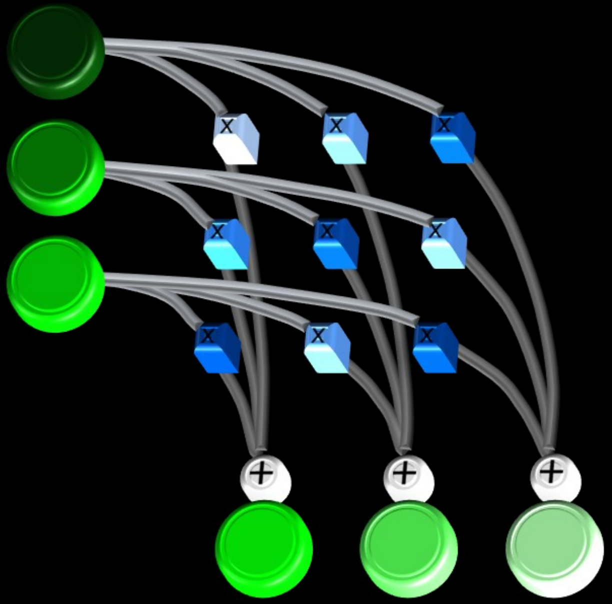
At each layer, a matrix vector multiplication is performed. “Learning” is achieved by adjusting the matrix elements, by analogy: the synaptic weights

$$\begin{bmatrix} a & b & c \\ d & e & f \\ g & h & i \end{bmatrix} \cdot \begin{bmatrix} x \\ y \\ z \end{bmatrix} = \begin{bmatrix} ax + by + cz \\ dx + ey + fz \\ gx + hy + iz \end{bmatrix}$$

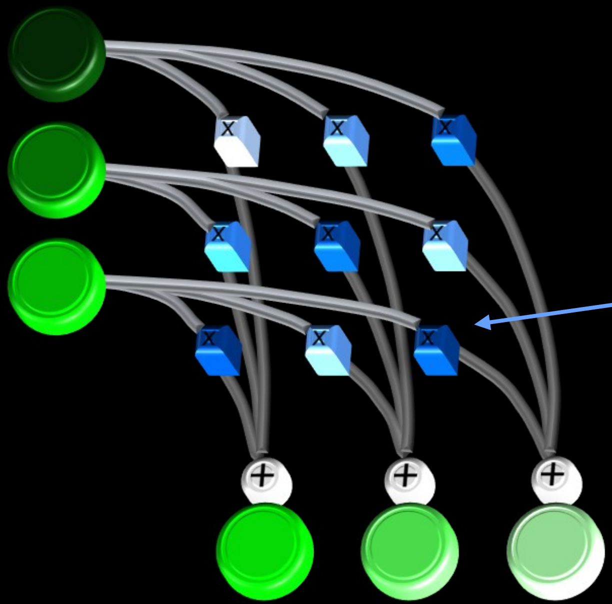




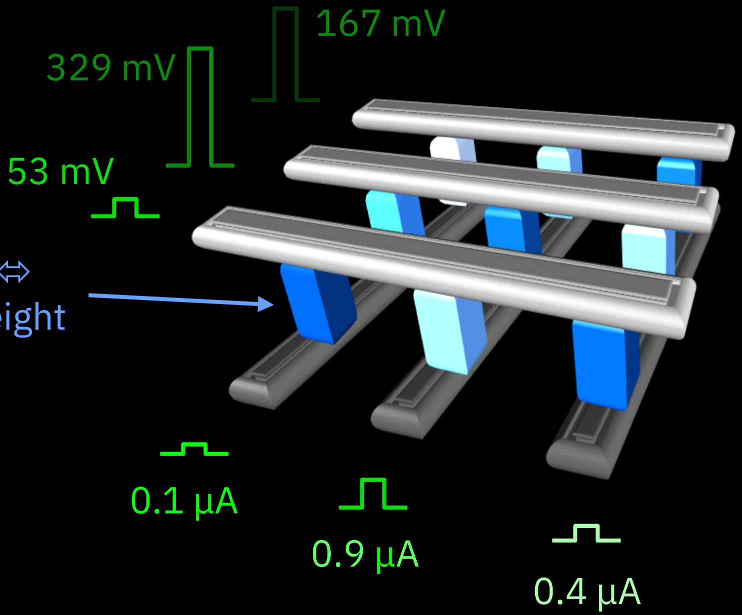
Accelerating Artificial Neural Networks: We aim at implementing matrix-vector multiplication in an analog way.



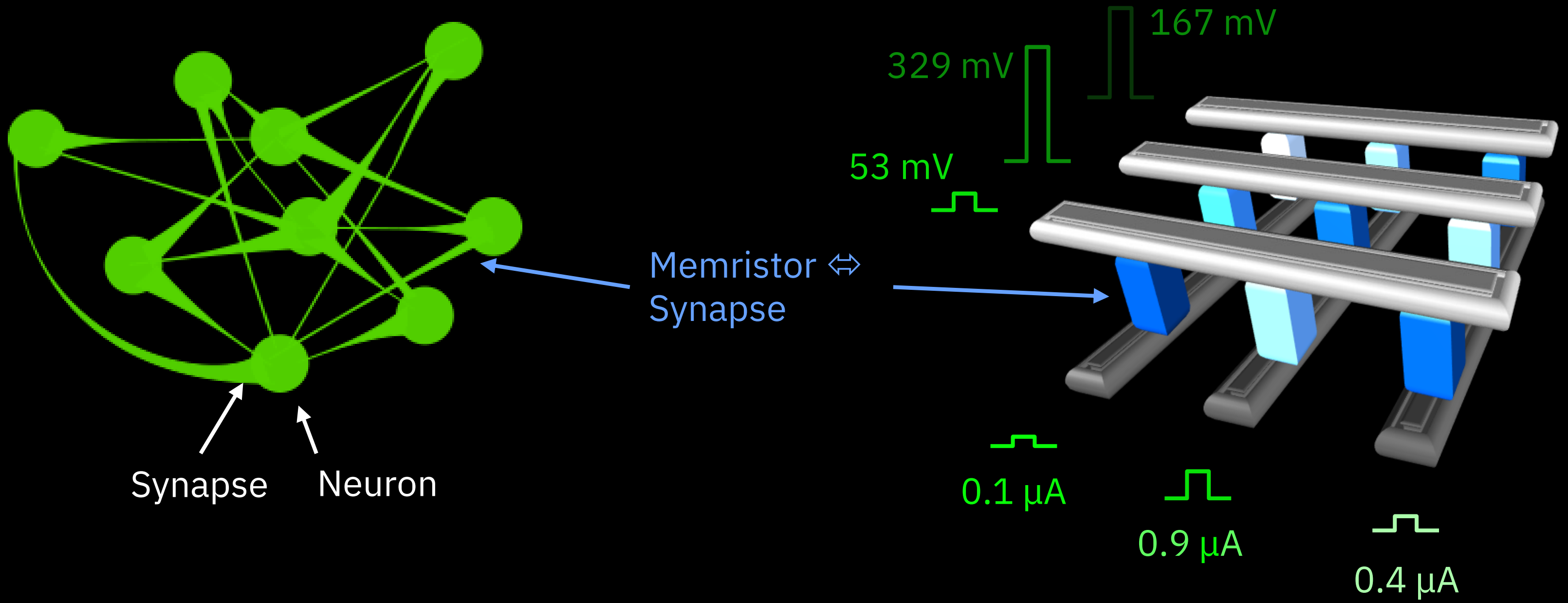
Analog multiplication:
Parallel voltage drop through a cross-bar arrays of resistances



Resistance ⇔
Synaptic weight



Analog multiplication in an Artificial Neural Network: Tuneable resistance + memory = “Memristor”



Motivation

Memristive ferroelectric junction

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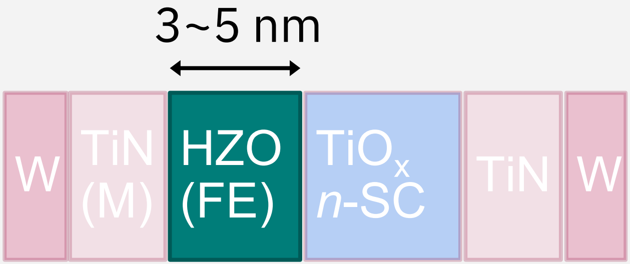
Memristive Ferroelectric Tunnel Junctions

Requirements :

- FE layer thin enough to conduct

$HfZrO_4$ dielectric layer:

- **thick enough to stabilize ferroelectricity**
- **thin enough to allow conduction**

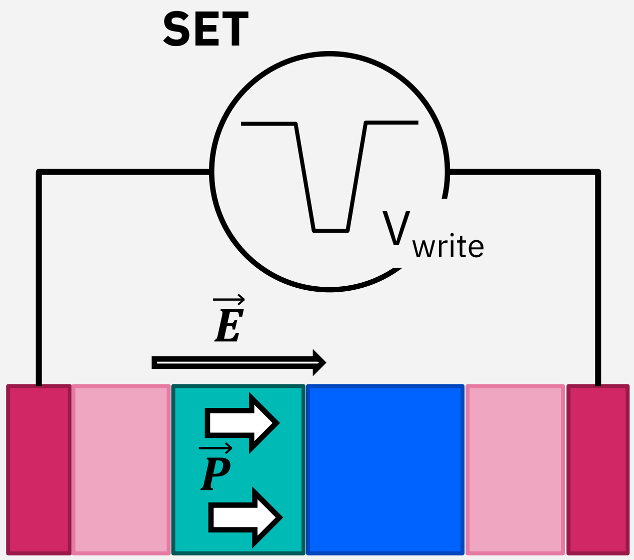


Memristive Ferroelectric Tunnel Junctions

Requirements :

- FE layer thin enough to conduct

- Coercive field of domains:
  - maximum: ⇔ to V_{write}~1-5 V (RE)SET pulses

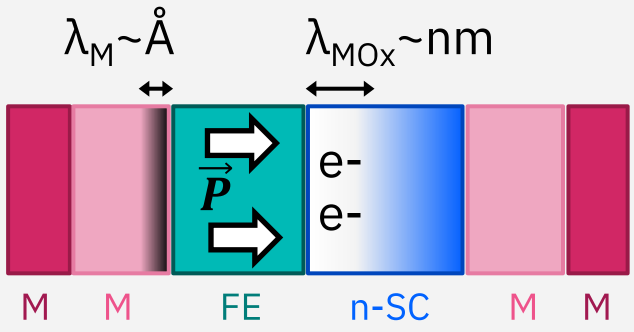


Memristive Ferroelectric Tunnel Junctions

Requirements :

- FE layer thin enough to conduct
- Coercive field of domains:
  - maximum: ⇔ to V_{write}~1-5 V (RE)SET pulses
- Carrier densities: $n_{SC} << n_M$

Screening of the ferroelectric polarization: λ ~ 1/n (n: carrier density)



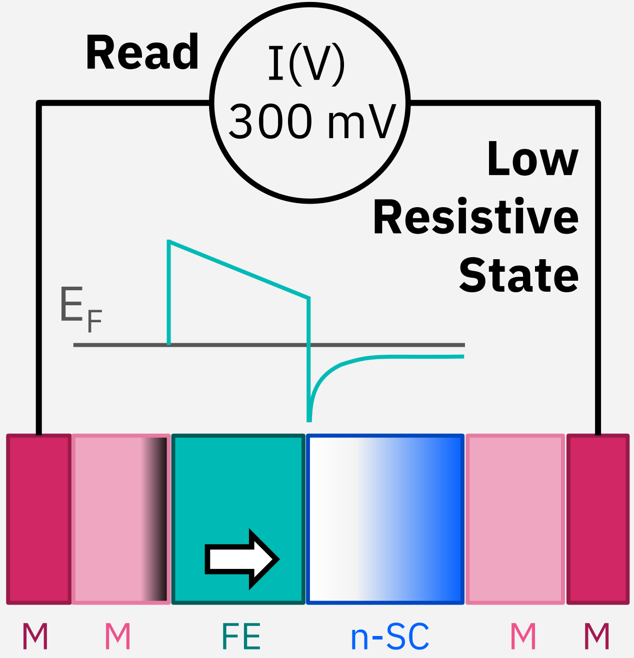
Memristive Ferroelectric Tunnel Junctions

Requirements :

- FE layer thin enough to conduct

- Coercive field of domains:
  - maximum: ⬄ to V_{write}~1-5 V (RE)SET pulses
  - minimum: ⬄ to > V_{read}~0.3 V

- Carrier densities: $n_{SC} << n_M$



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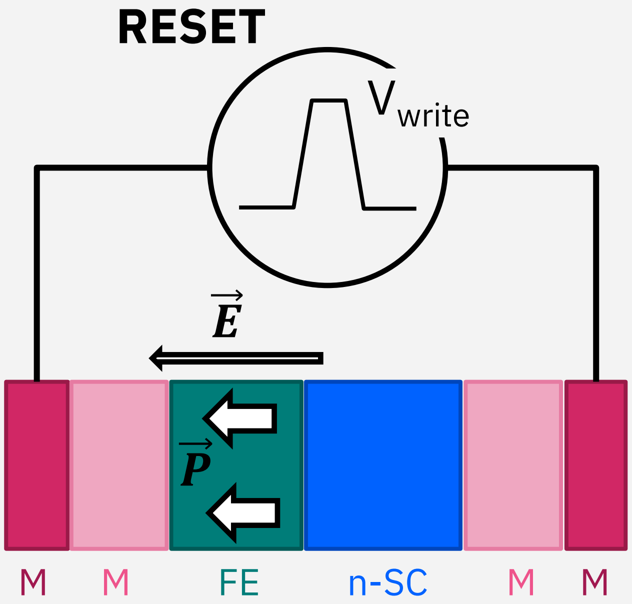

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Memristive Ferroelectric Tunnel Junctions

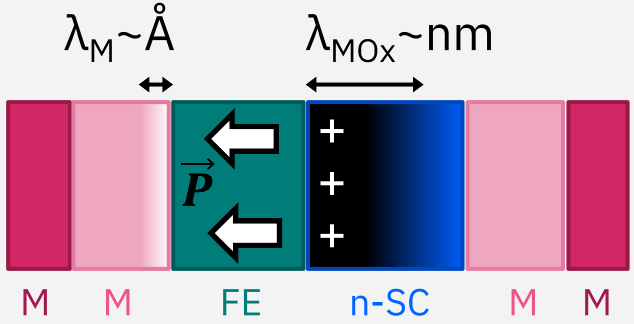
Requirements :

- FE layer thin enough to conduct
- Polarization is stable in both directions

- Coercive field of domains:
  - maximum: ⇔ to V_{write}~1-5 V (RE)SET pulses
  - minimum: ⇔ to > V_{read}~0.3 V

- Carrier densities: $n_{SC} << n_M$

Depletion of carriers at the FE/MOx (n-type) interface



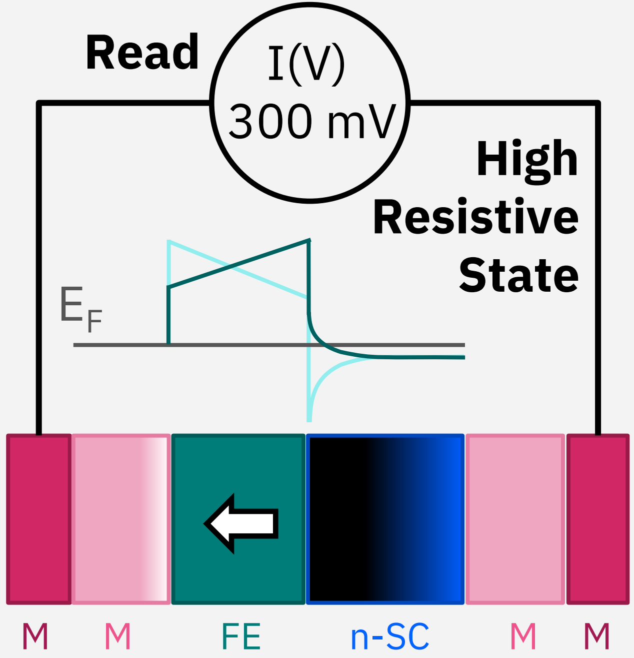
Memristive Ferroelectric Tunnel Junctions

Requirements :

- FE layer thin enough to conduct
- Polarization is stable in both directions
- Polarization is large enough to modify the energy profile

- Coercive field of domains:
  - maximum: ⇔ to V_{write}~1-5 V (RE)SET pulses
  - minimum: ⇔ to > V_{read}~0.3 V

- Carrier densities: $n_{SC} << n_M$



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Memristive Ferroelectric Tunnel Junctions

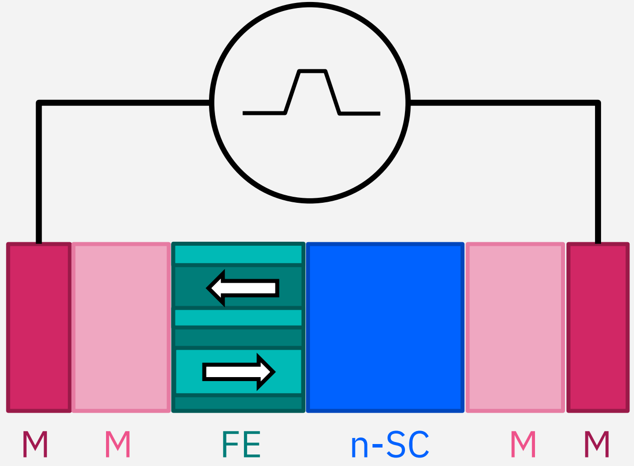
Requirements :

- FE layer thin enough to conduct
- Polarization is stable in both directions
- Polarization is large enough to modify the energy profile

- Coercive field of domains:
  - maximum: ⇔ to V_{write}~1-5 V (RE)SET pulses
  - minimum: ⇔ to > V_{read}~0.3 V
  - allow **intermediate configurations**

- Carrier densities: $n_{SC} << n_M$

Domains of different coercive fields enables analog switching



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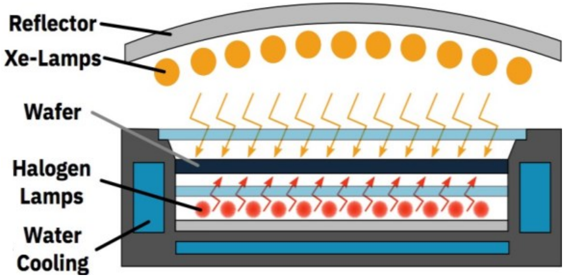
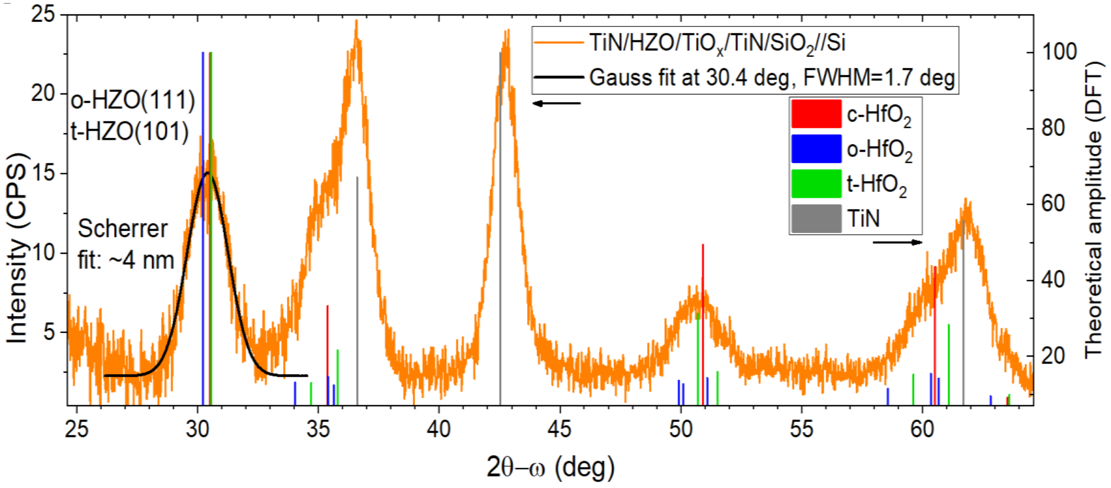
MFSM Stack, BEOL compatible process



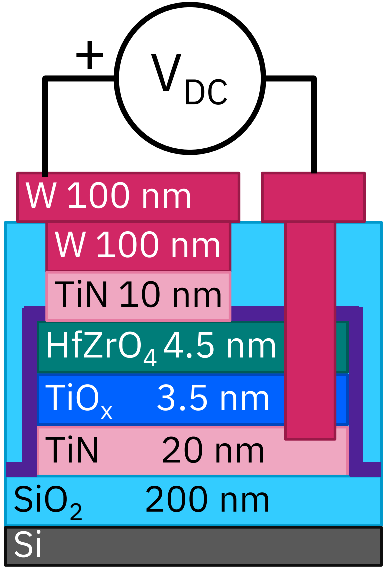
📖 É. O'Connor et al., APL Mater., vol. 6, no. 12, p. 121103, **2018**

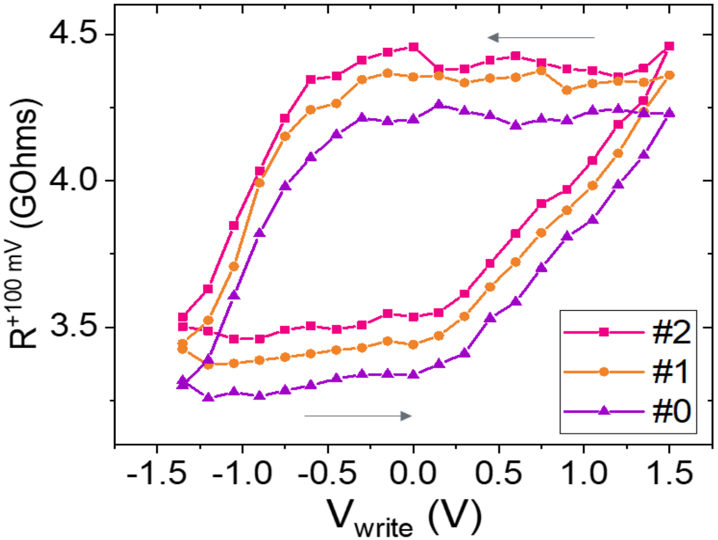


TiN	10 nm
$HfZrO_4$	4.5 nm
TiO_x	3.5 nm
TiN	20 nm
SiO_2	200 nm
Si	

- Atomic Layer Deposition of TiN, $HfZrO_4$ and TiO_x on a passivated surface
- ms-Flash Lamp Annealing process allows crystallization in o/t phase with reduced thermal budget (375C preheat + 70 J/cm^2)

Resistive switching in FTJ with TiOx interlayer





Ø 80 µm capacitors defined by optical lithography

1) apply a DC bias V_{write}
2) Set V to zero, wait
3) Measure the resistance at V_{read} = 100 mV
... repeat with different V_{write}

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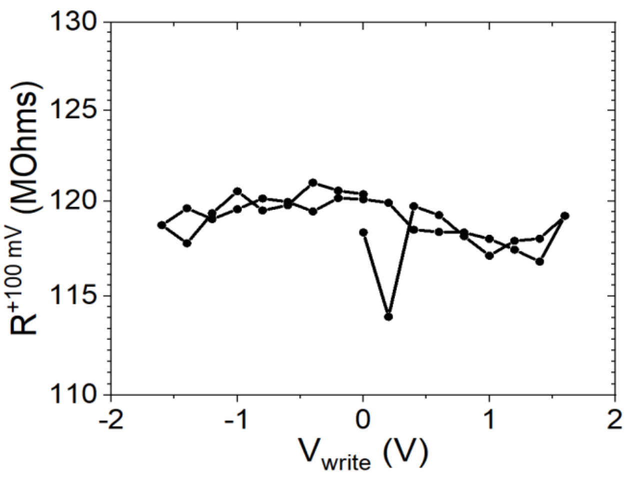
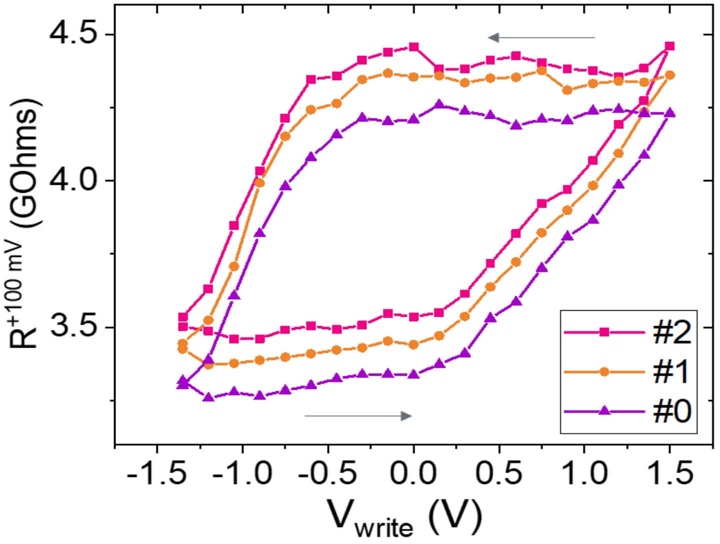
Resistive switching in FTJ with TiOx interlayer



Resistive switching not observed in similar structures with amorphous HZO



1) apply a DC bias V_{write}
2) Set V to zero, wait
3) Measure the resistance at V_{read} = 100 mV
... repeat with different V_{write}

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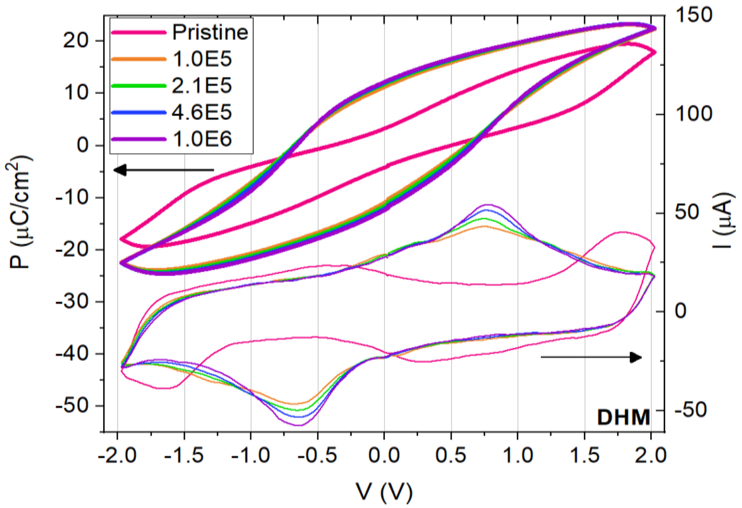
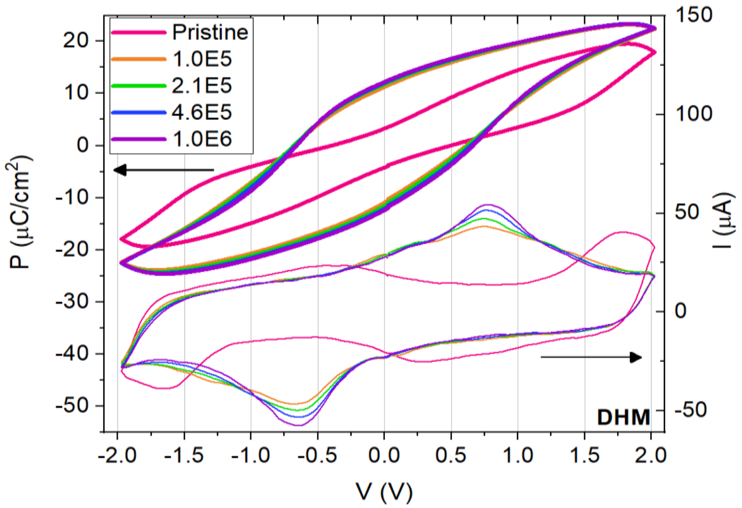
Wake-up effect in HZO layer

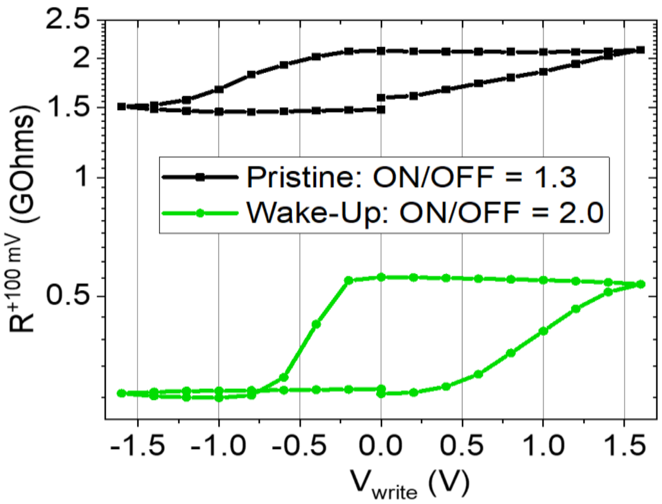


Fatigue: 100 kHz. 2 V.
Dynamic Hysteresis Measurements (DHM) show pristine: pinched loop then wake-up: FE loop

- Unpinning of ferroelectric domains
- Redistribution of oxygen vacancies

Wake-up effect in HZO layer





Fatigue: 100 kHz. 2 V.
Dynamic Hysteresis Measurements (DHM) show pristine: pinched loop then wake-up: FE loop

Increased ON/OFF after ferroelectric wake-up

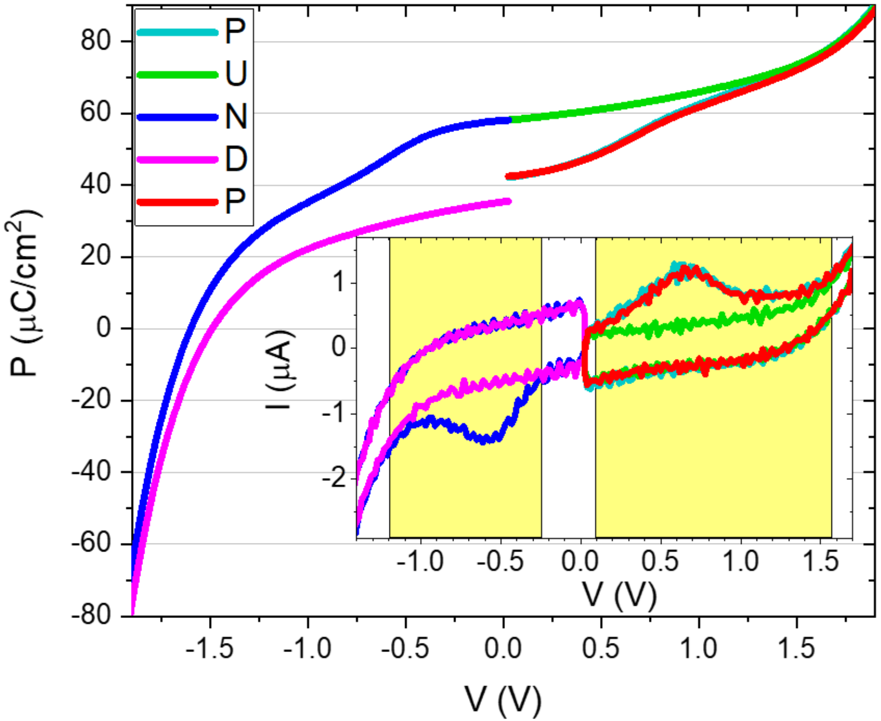
📖 Bégon-Lours *et al.*, Phys. Status Solidi RRL **2021**, 2000524

Resistive and FE switching in same voltage range

PUND after wake-up:
V<0 Narrow range
V>0 Wide range

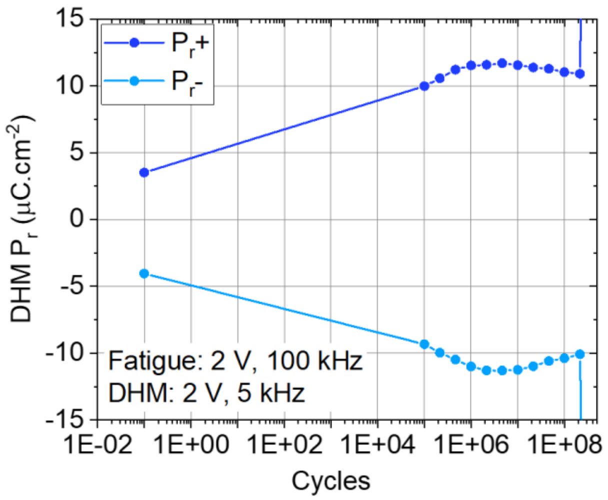
Matches the ranges where resistive switching is observed.

Demonstrates that resistive switching originates from ferroelectricity

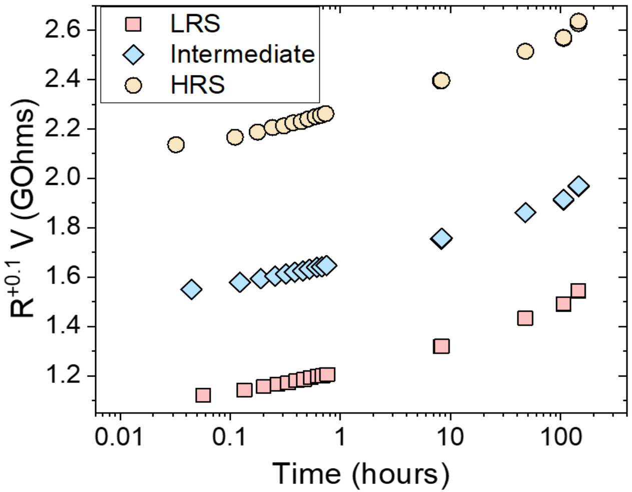


📖 Bégon-Lours *et al.*, Phys. Status Solidi RRL **2021**, 2000524

Endurance & Retention



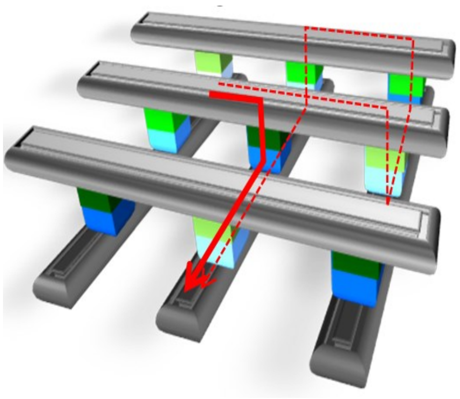
Fatigue measurements (100 kHz). Each data point corresponds to a DHM measurement at 2 V and 5 kHz. Leakage current result in overestimation of the polarization.

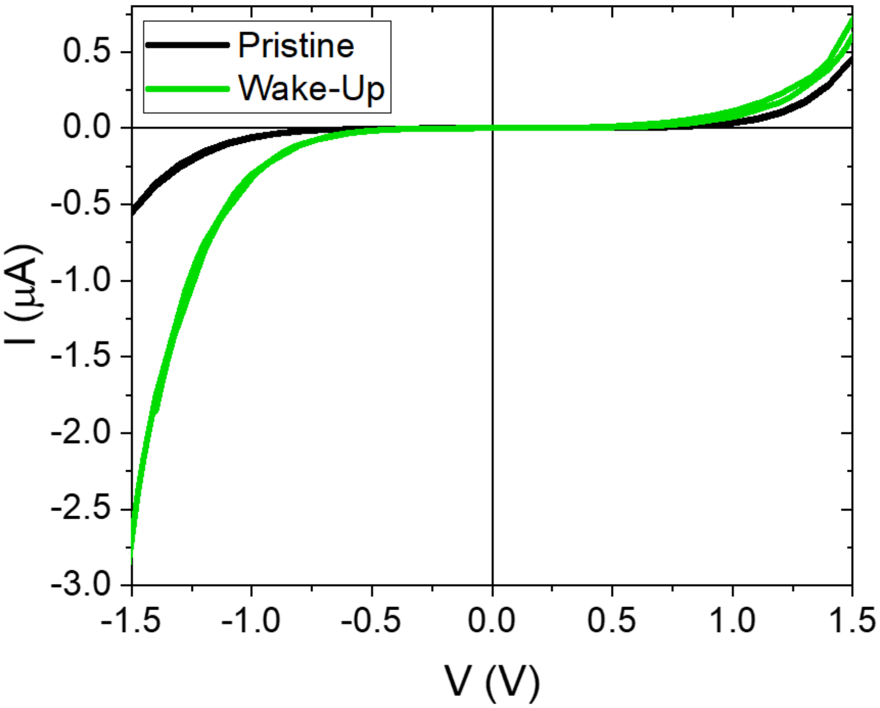


Retention of three devices in LRS, intermediate and HRS show drift but memory of the state

Ideal I-V: diode-like with linear regime

- Intrinsic diode-like: self-limits sneak paths in cross-bar arrays during weight update





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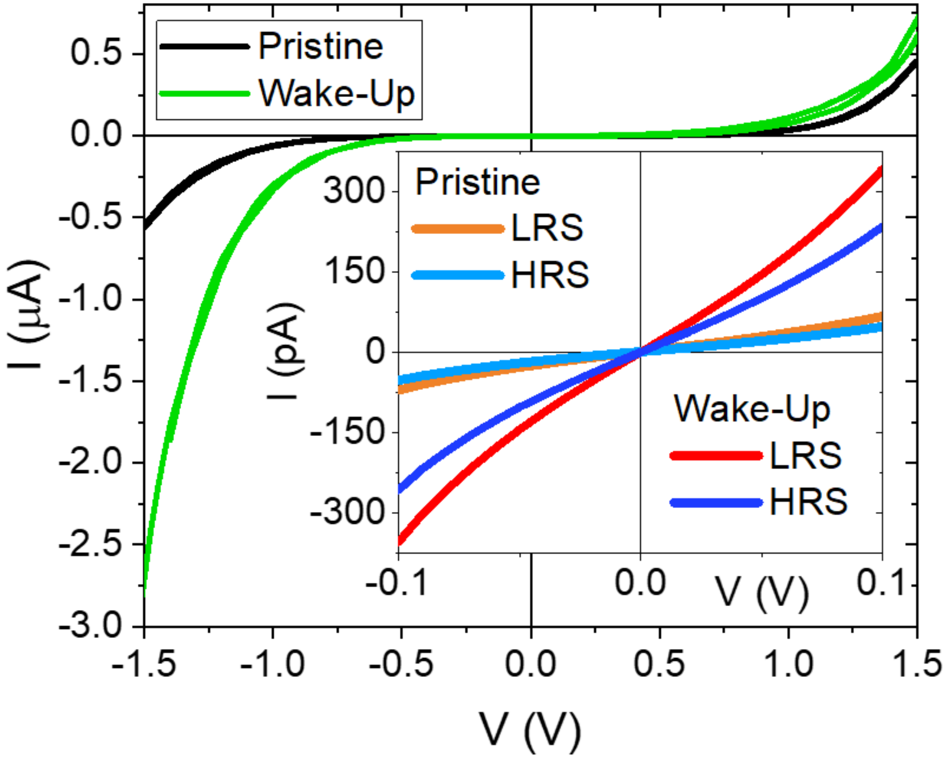
Ideal I-V: diode-like with linear regime

- Intrinsic diode-like: self-limits sneak paths in cross-bar arrays during weight update

- Quasi-linear regime around V_{read}: practical for Vector-Matrix-Multiplication



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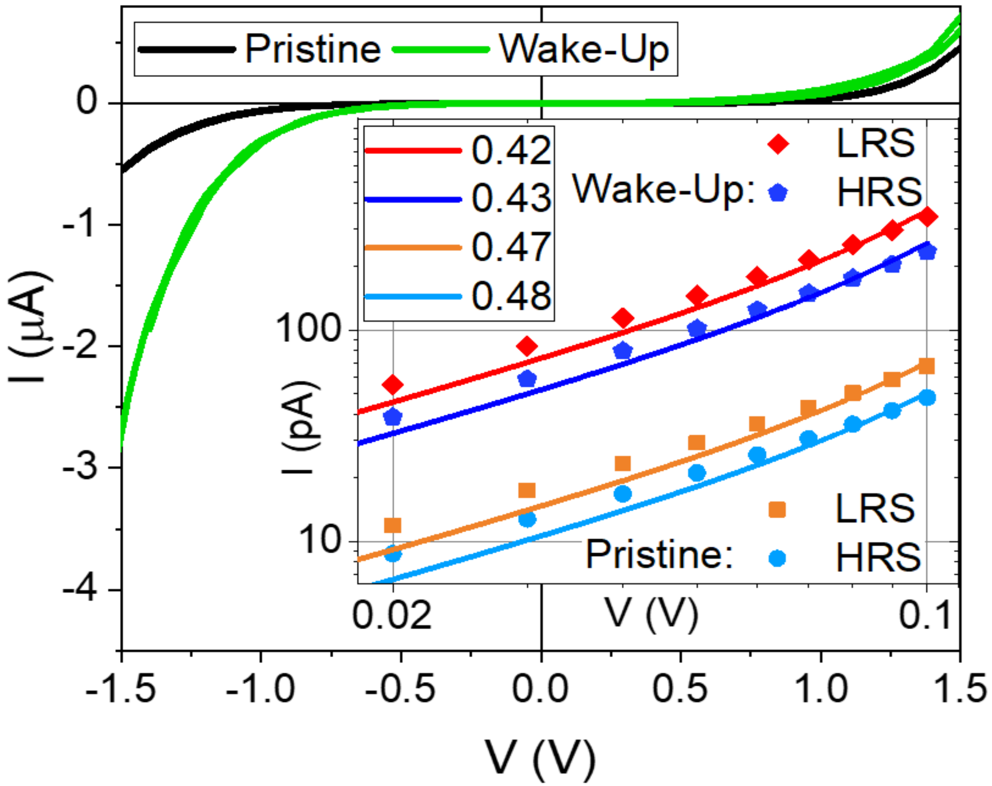
“Tunnel” Junction ?

Direct Tunneling model fitting: 0.4 eV
Brinkman model:

$$J \cong C\frac{\exp\left\{\alpha(V)\left[\left(\varphi_2-\frac{eV}{2}\right)^{3/2}-\left(\varphi_1+\frac{eV}{2}\right)^{3/2}\right]\right\}}{\alpha^2(V)\left[\left(\varphi_2-\frac{eV}{2}\right)^{1/2}-\left(\varphi_1+\frac{eV}{2}\right)^{1/2}\right]^2}\times \sinh\left\{\frac{3}{2}\alpha(V)\left[\left(\varphi_2-\frac{eV}{2}\right)^{1/2}-\left(\varphi_1+\frac{eV}{2}\right)^{1/2}\right]\frac{eV}{2}\right\} \quad (1)$$

where $C = -(4em)/(9\pi^2\hbar^3)$ and $\alpha(V) \equiv [4d(2m)^{1/2}]/[3\hbar(\phi_1 + eV - \phi_2)]$.

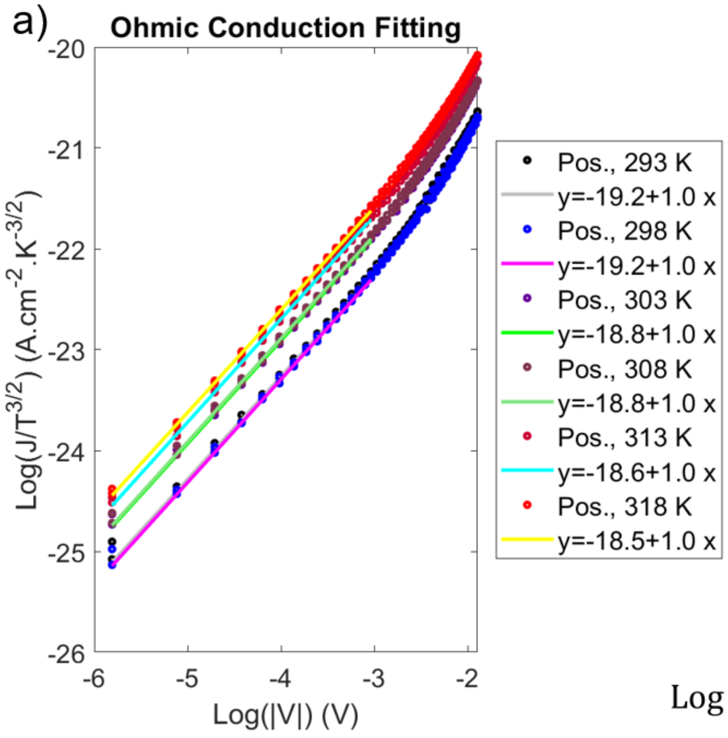
📖 A. Gruverman *et al.* *Nano Letters* **2009**, *9*, 3539.



red, resp. blue, orange and light blue lines represent calculated direct tunnel current with a symmetric barrier height of 0.42, resp. 0.43, 0.47 and 0.48 eV and a thickness of 4.5 nm, with the Brinkman model.

📖 Bégon-Lours *et al.*, Phys. Status Solidi RRL **2021**, 2000524

Ohmic conduction at low bias, temperature dependent



Temperature dependent measurements:

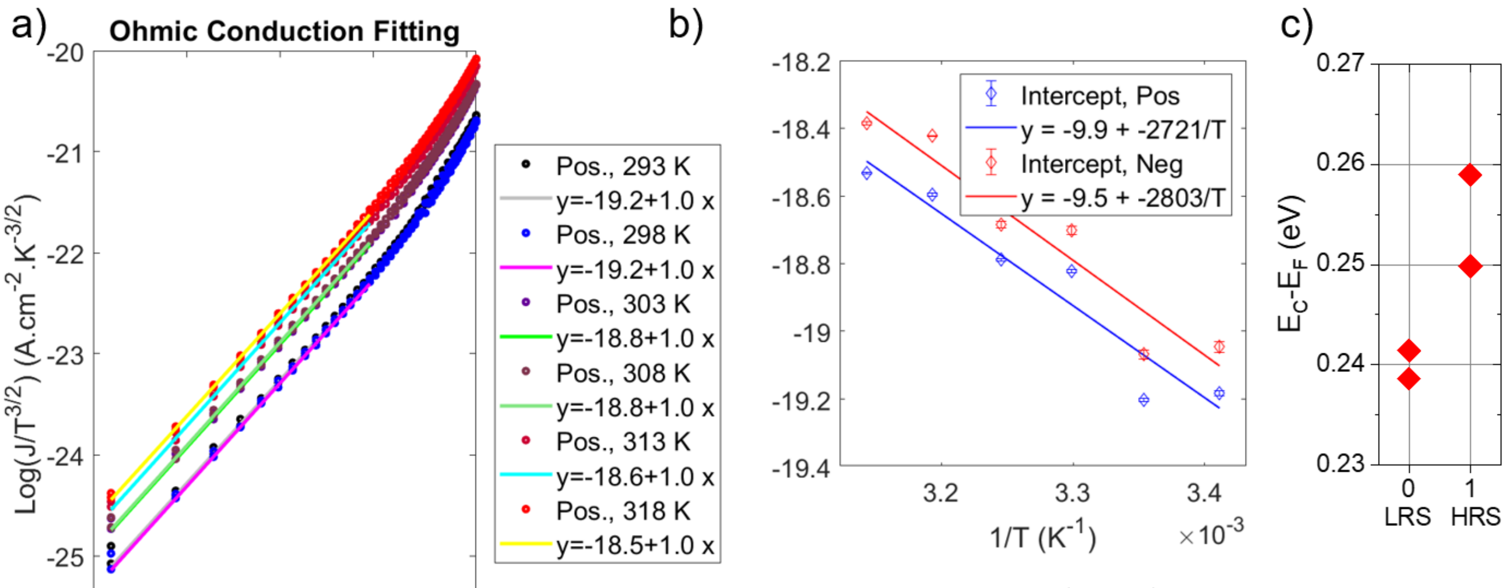
- R varies with T, discards direct tunneling

$$J = q\mu E N_C \exp\left[\frac{-(E_C-E_F)}{kT}\right] \quad \Leftrightarrow$$

$$\mathrm{Log}\left(\frac{J}{T^{\frac{3}{2}}}\right) = Log\left(q\mu\frac{N_C}{T^{\frac{3}{2}}}\right) + \frac{-(E_C - E_F)}{kT} + \mathrm{Log(E)}$$

📖 Bégon-Lours *et al.*, Phys. Status Solidi RRL **2021**, 2000524

Ohmic conduction at low bias, temperature dependent



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Temperature dependent measurements:

- R varies with T, discards direct tunneling
- E_C-E_F~0.25 eV confirms impurity level in the band gap of HZO

📖 Bégon-Lours *et al.*, Phys. Status Solidi RRL **2021**, 2000524

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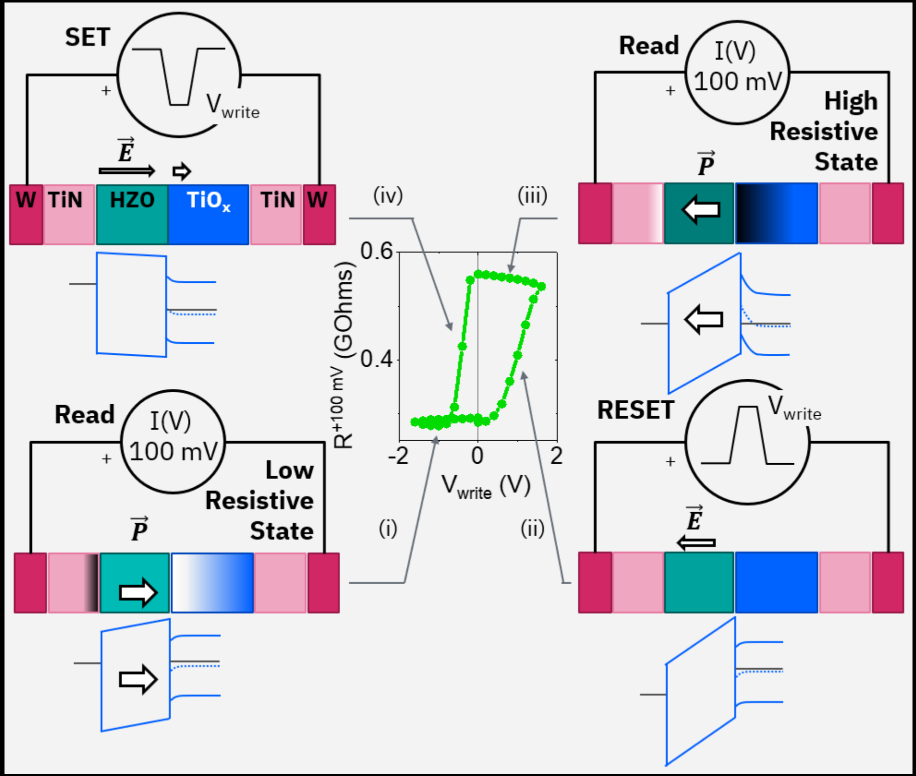
Conclusion

- Resistive switching observed in ultra-thin HZO junctions fabricated with a BEOl compatible process
- Origin of the resistive switching proved to be ferroelectricity
  - Linked to crystallinity
  - correlation between coercive field and resistive switching
  - Increased resistive switching upon FE wake-up
- Conduction does not occur by direct tunnelling but through a conduction band in HZO



📖 Bégon-Lours *et al.*, Phys. Status Solidi RRL **2021**, 2000524