Ferroelectric, Analog Resistive Switching in BEOL Compatible TiN/$HfZrO_4$/TiO_x Junctions

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***Abstract*— Thanks to their compatibility with CMOS technologies, hafnium based ferroelectric devices receive increasing interest for the fabrication of neuromorphic hardware. In this work, an analog resistive memory device is fabricated with a process developed for Back-End-Of-Line integration. A 4.5 nm thick $HfZrO_4$ (HZO) layer is crystallized into the ferroelectric phase, a thickness thin enough to allow electrical conduction through the layer. A TiO_x interlayer is used to create an asymmetric junction as required for transferring a polarization state change into a modification of the conductivity. Memristive functionality is obtained, in the pristine state as well as after ferroelectric wake-up, involving redistribution of oxygen vacancies in the ferroelectric layer. The resistive switching is shown to originate directly from the ferroelectric properties of the HZO layer.**

Keywords—memristors, hafnium zirconate, ferroelectrics

I. INTRODUCTION

Bio-inspired hardware accelerators supporting deep-learning are being developed [1], their building block is the memristor [2]. In a two-terminals ferroelectric memristor, a ferroelectric layer separates two different electrodes: upon polarization reversal, the energy profile and thus the transport probability of carriers across the ferroelectric layer is modified [3]. Their fabrication is challenging as the ferroelectric layer must be thick enough to stabilize ferroelectricity, but thin enough to allow electric conduction. In addition, Back-End-Of-Line (BEOL) processes not exceeding 400˚C are critical for industrializing beyond-Von-Neumann hardware in CMOS based silicon technology. The discovery of ferroelectricity in doped HfO_2 [4] enabled the demonstration of ferroelectric three terminals devices with BEOL compatible processes [5]. For two-terminals devices, reducing the thickness while keeping a low crystallization temperature is a critical aspect: HZO devices with <5 nm thicknesses have been obtained for processes above 450˚C [6], [7]. Devices with 10 nm thick layers can be crystallized at 400˚C [8], [9] but result in low current densities (<1 µA.cm^{-2} at 2 V). We demonstrate non-volatile analog resistive switching (memristive functionality) in a 4.5 nm thick ferroelectric layer in a BEOL compatible stack. We show that resistive switching is enhanced after wake-up and that it originates from the ferroelectric polarization.

II. NON-VOLATILE, ANALOG RESISTIVE SWITCHING

A TiN(10 nm)/HZO(4.5 nm)/TiOx(3.5 nm)/TiN (20 nm) asymmetric stack is deposited by Atomic Layer Deposition (ALD) on a SiO_2//Si substrate. The crystallization at a moderate thermal budget (~375˚C) is obtained using a ms-Flash Lamp Annealing (ms-FLA) [10]. X-Ray Diffraction shows HZO crystallized in the orthorhombic or tetragonal phase and that no fraction of monoclinic phase is found. A W electrode is then sputtered and circular capacitors then fabricated using standard optical lithography techniques.

To demonstrate memristive functionality of the resistive memory, we first apply "write" pulses of a voltage V_{write} across the device, while the bottom electrode (HZO/TiO_x/TiN interface) is grounded. The bias is then set back to zero, and, approximatively ten seconds later, the resistance is measured with a read voltage of 100 mV (non-destructive read-out). The results of this write/read experiment (black curve, pristine device) are plotted in **Figure 1**. After applying V_{write} = -1.5 V, the junction is in a Low Resistive State (LRS). Upon the application of pulses of increasing voltage, the resistance remains stable until it increases sharply at V_{write} = 0.3 V. The resistance then gradually increases (RESET), and the device reaches a High Resistive State (HRS). With pulses of decreasing voltage, the resistance remains stable until it decreases sharply at V_{write} = -0.45 V. A gradual decrease in resistance is then observed until it reaches its initial value (low resistive state, SET). In the conditions of the experiment, a moderate drift of the LRS is observed (a few tens of kOhms from cycle to cycle). A drift is also observed on a longer timescale: three devices poled in the LRS, HRS and in an intermediate state all see their resistance increase by 0.5 GOhms after six days, the memory of the state (LRS, HRS or intermediate) is preserved. The experiment demonstrates the non-volatile, analog, reversible resistive switching in the 4.5 nm thick HZO device.

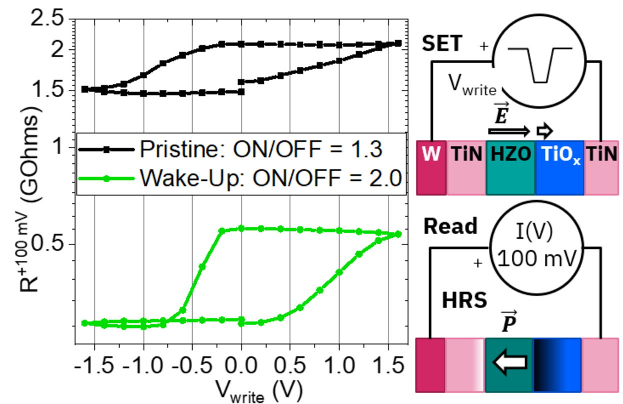

Figure 1. Resistance of pristine device (black curve) and after wake-up (green curve), measured at 100 mV, after applying a bias V_{write}. The TiO_x layer is grounded. The device stack, SET and read operations are sketched.

Capacitors of various sizes (40 to 140 µm) were measured. The constant current density and ON/OFF indicates that the conduction is homogeneous and not due to the formation of a filament through the HZO. Devices with amorphous HZO did not show resistive switching. Temperature dependent I-V

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characteristics show Ohmic conduction at small bias (V<50 mV). The conduction band is at 0.24 eV above the Fermi level in the LRS and 0.26 eV in the HRS, explaining the observed resistive switching. This value of energy difference between the conduction band and the Fermi level is small compared to the band gap of HZO (~3.5 eV) which indicates the presence of an impurity level in the band gap, from which the electrons are excited. At larger bias the I-V are non-linear, which is of technological interest: in selector-less cross-bar arrays, it can prevent current sneak paths through unselected devices.[11]

III. Improved Resistive Switching with Wake-up

Figure 2 shows Dynamic Hysteresis Measurements (DHM) of an 80 µm diameter device during wake-up (2 V, 100 kHz). The pristine loop is pinched and the remnant polarization is $2P_r = 7.5\ \mu C\cdot cm^{-2}$. After 1E5 cycles, the polarization increases to $2P_r = 24.6\ \mu C\cdot cm^{-2}$. For the pristine device, the switching current is maximal at -1.6 V and 1.8 V. These values then reduce to -0.7 V and 0.7 V, due to unpinning of ferroelectric domains during wake-up [12].

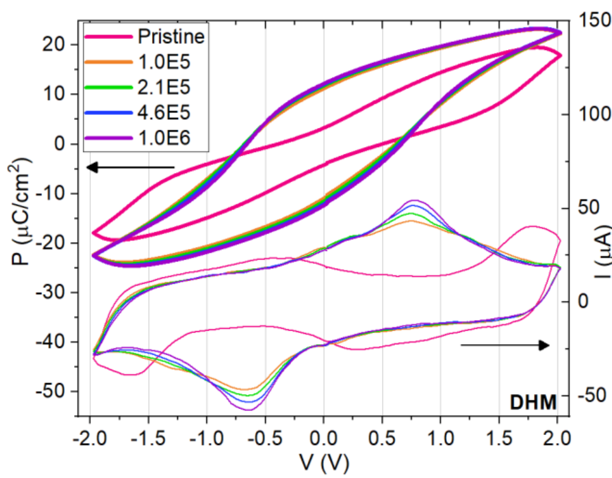

Figure 2: DHM polarization (left axis, thick lines) and current (right axis, thin lines) during wake-up (100 kHz, 2 V). Legend: number of cycles

The resistance measured at 100 mV for varying V_{write} bias before and after the wake-up is shown in **Figure 1**. After wake-up the resistance in the LRS decreases by a factor 5 and the ON/OFF ratio increases from 1.3 to 2.0. In section 2, we established the existence of an impurity level in the gap of HZO, which could be due to oxygen vacancies [13]: the two effects can be explained by the redistribution of oxygen vacancies during wake-up from the interface to the bulk of the HZO layer [14].

Figure 3 shows Positive Up Negative Down (PUND) measurements on the woken-up devices: the ranges within which resistive switching is observed (in **Figure 1**) correspond to the switching current (yellow regions in the inset showing the current as a function of the voltage: [-1.2 V;-0.2 V] and [0.1 V;1.6 V]), confirming the ferroelectric origin of the resistive switching.

The proposed mechanism is the following. Oxygen deficient TiO_x is a n-type semiconductor. The carrier density in the TiO_x layer is lower than in the metallic TiN: the screening of the polarization occurs over a larger distance. When the ferroelectric layer is polarized towards the TiO_x layer,

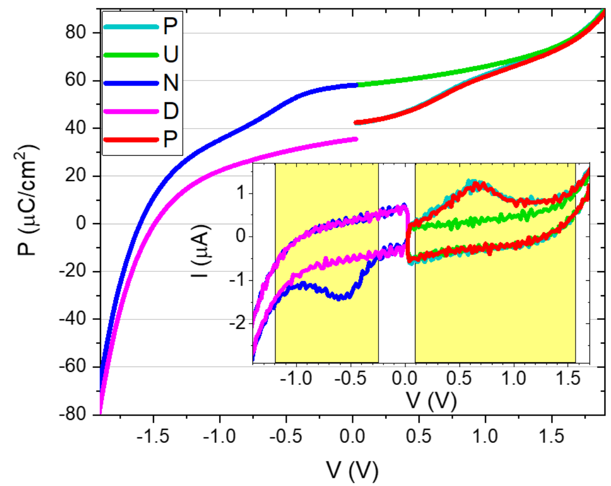

Figure 3. PUND measurements (100 Hz, 2 V, 5 ms) after wake-up: polarization versus voltage. Inset: current versus voltage.

electrons screen the ferroelectric polarization and accumulate in the TiO_x layer, which therefore becomes more conducting (low resistive state). When the ferroelectric polarization outwards the TiO_x layer two effects can explain the high resistive state: on one hand, the TiO_x layer is depleted near the HZO interface, which increases the thickness of the insulating barrier. On the other hand, the polarization field increases the energy barrier height at the TiO_x/HZO interface. Intermediate states are reached upon switching only a fraction of domains.

IV. Conclusion

Analog resistive memories were fabricated with a BEOL compatible process. Ferroelectricity was obtained in a 4.5 nm thick HZO layer crystallized with a moderate thermal budget of ~375°C. A TiO_x interlayer was used to create an asymmetry in the energy profile of a TiN/HZO/TiN capacitor. The memristive functionality (non-volatility and plasticity) was further enhanced after a ferroelectric wake-up of the devices. Electrical characterization confirms that the resistive switching originates from the ferroelectric properties of the HZO layer. These preliminary results raise interest in further understanding the role of the oxygen vacancies in the conduction mechanisms and the polarization to enhance the memristive functionality of HZO devices.

Acknowledgment

This work is funded by H2020: FREEMIND (840903), ULPEC (732642) and BeFerroSynaptic (871737).

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