Variability-Aware Read and Write Channel Models for 1S1R Crossbar Resistive Memory with High Wordline/Bitline Resistance

Zehui Chen and Lara Dolecek
Department of Electrical and Computer Engineering - University of California, Los Angeles
chen1046@ucla.edu, dolecek@ee.ucla.edu

***Abstract*—As technology scales down to single-nm regime, the increasing resistivity of wordline/bitline becomes a limiting factor to device reliability. This paper presents write/read communication channels while considering the line resistance and device variabilities by statistically relating the degraded write/read margins and the channel parameters. These models provide quantitative tools for evaluating the trade-offs between memory reliability and design parameters, such as array size, technology nodes, and aspect ratio, and for designing coding theoretical solutions for crossbar memory.**

I. Introduction

The crossbar resistive memory, whereby bistable memristors are placed at the crosspoint of wordlines and bitlines, is one promising candidate for the next generation nonvolatile memory due to its inherent $4F^2$ device density and its simple crossbar structure. Meanwhile, as technology scales down to single-digit-nm, simultaneously scaled wordline/bitline resistance increasingly becomes a limiting factor to device reliability and hence memory scalability [1].

The degradation of the write and read margins due to high line resistance are studied in [1], [2], [3]. Despite intensive research on this issue, it remains unclear how the degraded write/read margin affects the system level reliability metric, e.g., the bit-error rate (BER). Therefore, a study on the write and read channel models while considering the high line resistance could be beneficial for system engineers and error correction code (ECC) designers when designing next generation storage systems.

Previous studies on the write/read margin assumes deterministic High Resistance State (HRS) and Low Resistance State (LRS) whereas the HRS and LRS are nondeterministic in nature [4]. A study on the write/read channel models, which is done probabilistically, allows us to take the resistance variability of LRS and HRS into consideration for more precise modeling.

With line resistance, the write margins of cells are nonuniform across the array [3]. This non-uniformity can be leveraged to design ECC with higher efficiency. In [5], the authors designed non-stationary polar codes targeting non-uniform BER by characterizing the non-uniformity empirically. A theoretical characterization of the non-uniform channel properties also provide quantitative tools for more ECC works in a similar direction.

We enlist our main contributions in this work:

- Binary Asymmetric Channel models for writing to and reading from memory devices in crossbar memory, parameterized by device parameters, array size, wordline/bitline resistance and device location.
- Incorporation of non-deterministic HRS and LRS in the reliability analysis.
- Capacity results for crossbar resistive memory while considering the high line resistance.

Due to limited space, the following sections are shortened from our long version [6]. We refer readers to the long version for detailed background and detailed derivation of equations.

II. Background

For the write operation, we consider the V/2 write scheme, where wordline and bitline are biased at $1/2$ of the write voltage and 0, respectively, as it is usually more energy-efficient than the V/3 write scheme. For the read operation, we consider the current-mode sensing scheme as it has a smaller latency compared with the voltage-mode sensing scheme [2]. We focus on crossbar resistive memory with the widely used 1 selector 1 resistor (1S1R) structure, where highly nonlinear selectors are connected in series with the memristors to prevent write and read disturbs. The switching of memristor is stochastic and we model the switching time distributions as log-normal distributions according to [7]. The resistance of each state is also highly non-deterministic [4]. We assume the random variables, which represent the resistance of the cells, are i.i.d. and their conditional distributions, conditioned on the their states, are also log-normal distributions.

III. Channel Models

The channel models are depicted in Fig. 1. We discuss in the following subsections how the channel parameters are related to device parameters (μ_L, σ_L, μ_H and σ_H for the resistance distributions and t_{set}/t_{reset} for the switching distributions), line resistance (r_w and r_b) and device location (i, j).

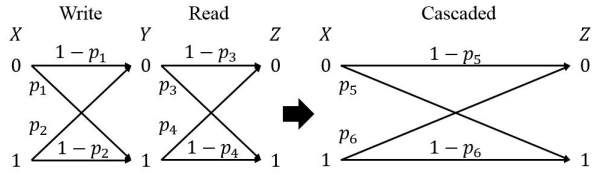


Fig. 1: Channel Models

A. Write Channel

Let the previous state of cell (i, j) be S^*_{ij} and the associated resistance value be R^*_{ij} with realization r^*_{ij}. A state switching is required when $S^*_{ij} \neq X_{ij}$. Due to high line resistances, the effective write voltage ($\tilde{V}_w(r^*_{ij}, i, j)$) applied on this cell could be much smaller than the desired write voltage. By considering the switching time distributions with switching time t_{set}/t_{reset} and the resistance distributions, we get:

$$P(Y_{ij}=0|X_{ij}=1,S^*_{ij}=0)=\int_{-\infty}^{\infty}\frac{1}{\sqrt{2\pi}r^*_{ij}\sigma_H}\times\exp\left[-\frac{\left(\ln r^*_{ij}-\mu_H\right)^2}{2\sigma_H^2}\right]Q\left(\frac{\ln t_{set}-\ln(\tau^{(ij)}_{set})}{\sigma_{set}}\right)dr^*_{ij}, \quad (1)$$

where $\tau_{set}^{(ij)}$ is dependent on $\tilde{V}_w(r_{ij}^*, i, j)$ with details in [6]. $P(Y_{ij} = 1|X_{ij} = 0, S_{ij}^* = 1)$ can be derived similarly. We therefore have the channel parameters as follows: $p_1^{(ij)} = (1 - q)P(Y_{ij} = 1|X_{ij} = 0, S_{ij}^* = 1)$, and $p_2^{(ij)} = qP(Y_{ij} = 0|X_{ij} = 1, S_{ij}^* = 0)$, where $q = P(X_{ij} = 0)$.

B. Read Channel

When using a threshold detector with threshold current I_{th} and read voltage V_r, we get the following closed form expressions for the channel parameters when we consider ideal selectors:

$$p_3^{(ij)} = Q\left(\frac{\mu_H - \ln\left(\frac{V_r}{I_{th}} - ir_w - jr_b\right)}{\sigma_H}\right), \tag{2}$$

and

$$p_4^{(ij)} = Q\left(\frac{\ln\left(\frac{V_r}{I_{th}} - ir_w - jr_b\right) - \mu_L}{\sigma_L}\right). \tag{3}$$

C. Cascaded Channel and Channel Capacity

The parameters of the cascaded channel readily follows: $p_5^{(ij)} = p_1^{(ij)}(1 - p_4^{(ij)}) + (1 - p_1^{(ij)})p_3^{(ij)}$ and $p_6^{(ij)} = p_2^{(ij)}(1 - p_3^{(ij)}) + (1 - p_2^{(ij)})p_4^{(ij)}$. The capacity of this cascaded channel for cell (i, j) is:

$$\begin{aligned} C_{ij} = \max_q \Bigg[& h\left(q\left(1 - p_5^{(ij)}\right) + (1 - q)p_6^{(ij)}\right) \\ & - qh\left(p_5^{(ij)}\right) - (1 - q)h\left(p_6^{(ij)}\right)\Bigg], \end{aligned} \tag{4}$$

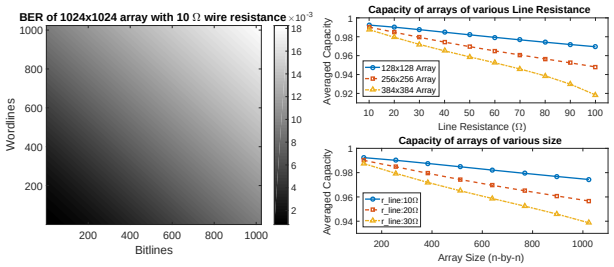
where $h(\cdot)$ is the binary entropy function. With near ideal selectors, the channel parameters for different cells in an array are independent, and we get the capacity of the whole array as: $C_{array} = \sum_{i,j} C_{ij}$.

IV. Simulations Results

We simulate multiple arrays to explore how memory parameters affects the memory reliability metrics, such as the bit-error rate (BER) and the averaged capacity. Parameters used in our simulation are summarized in Table I in [6].

In Fig. 2(a), we present the BER of each cell in a 1024×1024 array to illustrate the spacial variation of reliability. According to [1], the chosen 10Ω line resistance corresponds to the resistance per junction of Cu wire with 20nm technology nodes. With this moderate line resistance, we observe an order of magnitude BER difference between the best-case cell, located closest to the voltage source, and the worst-case cell, located furthest from the voltage source. The cell which is further from the source and sensing amplifier, suffers from a lower voltage delivery during the write operation and a higher accumulated line resistance during the read operation, thus has a larger BER.

Next, in Fig. 2(b), we present the averaged capacity per cell for arrays with various sizes and line resistances. We observe that a larger line resistance, which corresponds to a smaller technology node, deteriorates the averaged capacity almost linearly. This trade-off thus must be taken into consideration when scaling the memory, as it is shown in [1] that the line resistance scales exponentially with respect to the technology node. From Fig. 2 (b), we notice that the averaged capacity also deteriorates almost linearly, with respect to the array size. This effect is thus a limiting factor for the realization of a large memory array.



(a) Heatmap of BERs for a 1024x1024 array

(b) Capacity results with various sizes and line resistances

Fig. 2: Simulation Results

Array Size	128×128	64×512	32×512
Averaged Capacity	0.9924	0.9918	0.9897
Array Size	16×1024	8×2048	4×4096
Averaged Capacity	0.9845	0.9745	0.9573

TABLE I: Capacity of arrays with different aspect ratios

We further investigate how aspect ratio affects the averaged capacity by simulating arrays with the same number of cells but different aspect ratios. In Table I, the square array (aspect ratio = 1) has the largest averaged capacity and the 4×4096 array, which has the largest aspect ratio, has the lowest averaged capacity. This observation presents a trade-off between the sometimes desired high aspect ratio and a high averaged capacity for memory designers.

V. Conclusion and Future Works

In this paper, we proposed the read and write channel models for the 1S1R crossbar resistive memory while considering the nondeterministic nature of the memory device. Future research is in the direction of leveraging the channel information to improve memory reliability. This includes system level approaches such as finding the optimal read threshold and coding theoretic approaches such as designing time-varying LDPC codes with unequal bit protection capability.

Acknowledgment

Research supported in part by a grant from UC MEXUS and an NSF-BSF grant no.1718389.

References

[1] J. Liang *et al.*, "Effect of wordline/bitline scaling on the performance, energy consumption, and reliability of cross-point memory array," *ACM Journal on Emerging Techno. in Computing Systems (JETC)*, vol. 9, no. 1, p. 9, 2013.

[2] P.-Y. Chen, Z. Li, and S. Yu, "Design tradeoffs of vertical rram-based 3-d cross-point array," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 24, no. 12, pp. 3460–3467, 2016.

[3] A. Chen, "A comprehensive crossbar array model with solutions for line resistance and nonlinear device characteristics," *IEEE Trans. Electron Devices*, vol. 60, no. 4, pp. 1318–1326, 2013.

[4] B. Ji *et al.*, "In-line-test of variability and bit-error-rate of hfox-based resistive memory," in *2015 IEEE International Memory Workshop (IMW)*. IEEE, 2015, pp. 1–4.

[5] M. Zorgui *et al.*, "Polar coding for selector-less resistive memories," in *10th Annual Non-Volatile Memories Workshop*, San Diego, CA, Mar. 2019.

[6] Z. Chen and L. Dolecek, "Variability aware read and write channel models for 1s1r crossbar resistive memory with high wordline/bitline resistance," 2019, http://arxiv.org/abs/1912.02963.

[7] Medeiros-Ribeiro *et al.*, "Lognormal switching times for titanium dioxide bipolar memristors: origin and resolution," *Nanotechnology*, vol. 22, no. 9, p. 095702, 2011.