

Coding Assisted Adaptive Thresholding for Sneak-Path Mitigation in Resistive Memories

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Abstract—In crossbar resistive memory, the sneak-path problem is one of the main challenges for reliable readout. The sneak-path event can be described combinatorially and its adverse effect can be modeled as a parallel interference. In this work, based on a high-rate coding scheme, we characterize the inter-cell dependency of sneak-path events probabilistically. Utilizing this characterization, we present adaptive thresholding schemes for resistive memory readout using side information provided by precoded bits. This estimation theoretic approach effectively reduces the bit-error rate.

I. INTRODUCTION

Crossbar resistive memory, in which a memristor is positioned on each row-column intersection of the crossbar structure, is considered to be a promising candidate for future non-volatile memory device. One fundamental problem in resistive memory has attracted significant research attention is the *sneak-path* problem [1]. Sneak paths are undesirable paths in parallel to the selected cell and traverse through unselected cells. The current going through the sneak paths makes the read operation unreliable. This problem is especially severe when a cell in High-Resistance State (logic 0) is read because parallel low resistances, due to sneak-paths, lower the resistance measured from the cell at High-Resistance State, thus causing difficulties in distinguishing between the Low-Resistance State and the High-Resistance State.

In [2], the sneak-path problem is formulated as an *estimation problem*, and the effect of the sneak-path event is viewed as a *parallel interference*. In [3], the dependency of the sneak-path problem between two cells on the same row/column is studied. Motivated by these two previous works, we present adaptive thresholding schemes dependent on the side-information gathered through precoded bits, utilizing a high-rate coding construction and our probabilistic characterization of the inter-cell dependency. This is the first work that exploits the inter-cell dependency in resistive memory to improve estimation accuracy, i.e., to mitigate the adverse effect of the sneak-path problem. Simulation results show an order of magnitude improvement in terms of achieved bit-error rate.

II. SNEAK PATH MODELING AND THE DIAGONAL-0 CODING

A. Sneak path Modeling for 1T1R structure

As an initial step, we use the sneak-path definition in [3] with modification, and also restrict ourselves to a sneak-path of length 3. Other factors that affect the occurrence of a sneak-path, such as wire resistance, are not considered in this work and are left for future work. Our model further treats the crossbar resistive memory with 1D1R structure in which to each memristor cell, a selection device (a diode) is connected

in series with the memory cell. Our model assumes the diode fails i.i.d. with probability p_f due to reliability issue [2]. Note that this model can be easily extended to crossbar resistive memory without any selection device by setting $p_f = 1$. Let $A \in \{0, 1\}^{n \times n}$ denote the data matrix representing data stored in a crossbar resistive memory of size $n \times n$, and let A_{ij} denote the bit value at cell (i, j) . By our definition, a sneak-path event occurs at cell (i, j) for an array with the 1D1R structure if the following three conditions are met:

- 1) The bit value stored is 0.
- 2) There exists at least one combination of $c, r \in [1, \dots, n], c \neq j, r \neq i$ that induces a sneak-path defined by $A_{ic} = A_{rc} = A_{rj} = 1$.
- 3) The diode at cell location (r, c) fails to open position.

We define e_{ij} to be a boolean random variable denoting the occurrence of the sneak-path event at location (i, j) , conditioned on the bit value stored at (i, j) being 0 and we also refer to e_{ij} as the sneak-path state of cell (i, j) .

Our modeling of the adverse effect of a sneak-path event is adapted from [2]. We first define the 0/1 state resistance of memristor to be R_0/R_1 . We then denote r_{ij} to be the measured resistance value of cell (i, j) with a Gaussian measurement noise η with variance σ^2 [2]. The adverse effect of a sneak-path event is modeled as a parasitic resistor with value R_s that is parallel to the read cell. Together, we have the following model:

$$r_{ij} = \begin{cases} \left(\frac{1}{R_0} + \frac{e_{ij}}{R_s} \right)^{-1} + \eta & \text{when 0 is stored,} \\ R_1 + \eta & \text{when 1 is stored.} \end{cases} \quad (1)$$

B. The Diagonal-0 coding

In crossbar resistive memory, as noted in [3], it is not hard to observe that the occurrence of a sneak-path event at one cell is *not* independent of the occurrence of a sneak-path event at another cell. For example, knowing that $e_{ij} = 1$ increase the probability of $e_{ij'} = 1, j' \in [1, \dots, n], j' \neq j$, as well as $e_{i'j} = 1, i' \in [1, \dots, n], i' \neq i$. This special behavior of resistive memory presents natural difficulty to coding solutions when viewing the sneak-path event as a bit error. However, when viewing the effect of a sneak-path event as a parallel interference, one can utilize this inter-cell dependency to develop better estimation schemes based on side information provided by cells with known bit values. We thus present the following coding construction to better utilize this inter-cell dependency.

Construction 1. We defined A to be “diagonal-0” coded if A satisfy the following: $A_{ii} = 0, \forall i \in \{1, \dots, n\}$.

With this simple coding construction, each cell at location (i, j) , $(i \neq j)$, has one cell that stores a 0 in its row and another precoded 0 in its column. In this work, we restrict the resistive memory array to be square for simplicity.

III. PROBABILITIES AND JOINT PROBABILITIES OF SNEAK-PATH EVENT

In order to utilize the known 0s on the diagonal for more informed estimation schemes, several important probabilities need to be calculated analytically. First, in order to determine the sneak-path state of a precoded diagonal bit, we need $P(e_{ii})$. Second, in order to use the sneak-path state at diagonal cells for more informed estimation schemes, we need $P(e_{ij}|e_{ii}, A_{ij} = 0) = P(e_{ij}|e_{jj}, A_{ij} = 0)$ and $P(e_{ij}|e_{ii}, e_{jj}, A_{ij} = 0)$ for $i \neq j$. The two sets of conditional probabilities are used in different estimation schemes in the following section. To make a comparison with the scheme that does not use any side information, we also need $P(e_{ij}|A_{ij} = 0)$. In [4], we calculated these probabilities as a function of n based on the combinatorial characteristic of the sneak-path event. Due to space limitation, we omit these calculations here and direct readers to [4] for details.

IV. ADAPTIVE THRESHOLDING SCHEMES

We present two schemes, the *Double Threshold Scheme* based on single precoded 0 on the diagonal and the *Triple Threshold Scheme* based on two precoded 0s. For comparison, we also state the *Single Threshold Scheme* which uses no side information. For the two adaptive thresholding schemes, first we determine the sneak-path states of the precoded 0s on the diagonal, then based on these sneak-path states of the 0s, we choose appropriate thresholds to decide the states of the cells to be read. Thresholds for different conditions (sneak-path states) can be calculated based on the modeling in Section II and probabilities stated in Section III.

The optimal threshold (τ_s) for deciding the sneak-path state of a precoded cell is given by:

$$\tau_s = \frac{1}{2} \frac{R_0^2 - \left(\frac{1}{R_0} + \frac{1}{R_s}\right)^{-2} + 2\sigma^2 \log\left(\frac{P(e_{ii}=1)}{P(e_{ii}=0)}\right)}{R_0 - \left(\frac{1}{R_0} + \frac{1}{R_s}\right)^{-1}}. \quad (2)$$

We then calculate the optimal thresholds for the three thresholding schemes, assuming the sneak-path states of the precoded cells are known. The three thresholding schemes are alike and only differ on the side-information used for each scheme. Therefore, we use the variable c to denote the side-information used in each scheme collectively. We define $c = \{\}$ for the *Single Threshold Scheme*, $c = \{e_{jj}\}$ for the *Double Threshold Scheme*, and $c = \{e_{ii}, e_{jj}\}$ for the *Triple Threshold Scheme*. The corresponding optimal thresholds τ_c with some approximation are then:

$$\tau_c \approx \frac{1}{2} \frac{\left(\frac{1}{R_0} + \frac{1}{R_s}\right)^{-2} - R_1^2 + 2\sigma^2 \log\left(\frac{q}{(1-q)P(e_{ii}=1|A_{ij}=0,c)}\right)}{\left(\frac{1}{R_0} + \frac{1}{R_s}\right)^{-1} - R_1}. \quad (3)$$

In Equation (2) and (3), q is the prior probability that 1 is stored. The derivations of Equation (2) and (3) are omitted to save space and can be found in [4].

V. SIMULATION RESULTS

We evaluate the two adaptive thresholding schemes via simulation and compare the results with the *Single Threshold Scheme*. In the simulations, we use prior probability $q = 0.5$ and the following resistance values: $R_1 = 100\Omega$, $R_0 = 1000\Omega$, and $R_s = 250\Omega$, (same as [2]). We fix $p_f = 10^{-3}$ and $n = 8$

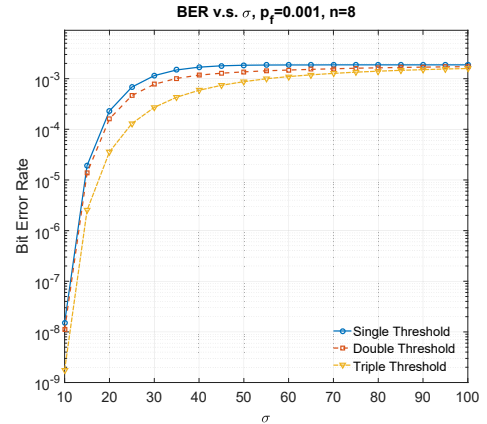


Fig. 1: BER of thresholding schemes at various noise levels

to study the influence of noise on the thresholding schemes. Figure 1 shows that both *Double Threshold Scheme* and *Triple Threshold Scheme* show notable improvements on BER in a noise regime of 20%–50% of R_1 . At low noise regime, while the *Double Threshold Scheme* shows similar performance as the *Single Threshold Scheme*, the *Triple Threshold Scheme* still shows an order of magnitude improvement. The two schemes both saturate together with the *Single Threshold Scheme* at very high noise level.

VI. CONCLUSION

In this work, utilizing the inter-cell dependency of sneak-path events, we provide a light-weight estimation theoretic scheme to mitigate the sneak-path problem in resistive memory. Our future work includes extending these schemes to consider arrays with non-unity aspect ratio and arrays with different selectors. This work can be also extended in many other directions. These adaptive thresholding techniques can be combined with constraint coding solutions to alleviate sneak-path problem in arrays without cell selectors. SPICE simulation with real memristor model can be also done to test our adaptive thresholding schemes.

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