Leveraging RAID for Soft BCH Decoding

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A. Abstract

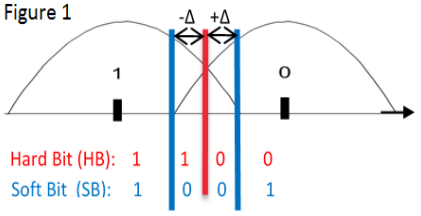
Storage Class Memory (SCM) is gaining increasing attraction in recent years as means to close the access time gap between memory and storage and enable next generation high performance computing and big data applications. One of the SCM challenges is enabling reliable, cost efficient, high performance storage in the presence of random errors and memory defects. Erasure codes, such as XORing across a Redundant Array of Independent Dies (RAID), are used for handling memory defects. Error Correction Codes (ECC) are used for handling random errors. Due to the high performance SCM requirements, low latency algebraic ECC solutions, such as BCH codes, are the preferred choice in SCM. Both the Erasure codes (i.e. XOR over RAID) and ECC require overprovisioning which effect the SCM cost efficiency. In this paper, we propose a scheme for significantly boosting the ECC correction capability by leveraging the existing XOR overprovisioning for enabling Soft BCH Decoding.

B. Background - Enabling reliable storage in the presence of random errors and memory defects

Ensuring data integrity and reliable storage over SCM requires protection against both random errors and memory defects. The random errors are handled using ECC schemes. The memory defects are commonly handled by XORing pages or sectors across different dies and storing the resulting XOR page on a separate die. This way, if a page is corrupted by a memory defect, it can be recovered by deXORing all the un-corrupted decoded pages within the XOR stripe from the XOR page. Both the ECC and the XOR scheme require overprovisioning on the SCM and hence effect its cost efficiency. It is desirable to minimize the overprovisioning that is required for ensuring reliable storage or to maximize the amount of errors that can be handled for a given allocated overprovisioning. The high performance and high Quality of Service (QoS) requirements of SCM, imply very harsh latency requirements for the SCM ECC solution. This means that state of the art, near Shannon limit performing, iterative ECC solutions, such as LDPC codes, are not applicable to SCM, due to their large code length and non-deterministic variable decoding latencies. Instead, it is customary to use Algebraic ECC solutions, such as short BCH codes, whose decoders have near deterministic very low decoding latencies. Unfortunately, BCH codes, cannot operate close to the Shannon limit and have relatively low correction capability for a given overprovisioning. One of the main reasons for the low correction capability of Algebraic ECC decoders is that they do not make use of “soft” information (except for high complexity and latency variants, e.g. Chase).

When reading a memory page, reliability information can be extracted on each of the read bits, by performing high resolution reads to identify the proximity of each memory cell’s current threshold to the memory state transition current. Such information, indicating the reliability of each read bit can serve as “soft” information that may be leveraged by a soft ECC decoder for significant increase in correction capability. Figure 1 shows an example of extracting “hard” and “soft” information during a memory read operation.

Figure 1



In this paper, we propose a scheme for significantly enhancing the correction capability of a conventional BCH decoder by leveraging the existing XOR overprovisioning for enabling Soft BCH Decoding.

C. Leveraging the XOR overprovisioning for Soft BCH Decoding

Conventionally, the two mechanisms, XOR scheme for NAND defects protection and ECC for random errors protection, operate independently each one utilizing its own parity overprovisioning.

This is sub-optimal. In cases where there is a high rate of random errors due to certain disturbance effects (such as temperature driven disturbs), then we may have multiple pages failing BCH decoding and also failing a recovery attempt using the XOR mechanism, as there may be more than one failing page within the XOR stripe. As a result, a conventional system would declare an uncorrectable page and data would be lost.

A more efficient approach would perform joint XOR and ECC decoding, leveraging the full allocated overprovisioning in order to boost the overall random errors correction capability. The idea is to combine the two sources, read ECC page from the memory and reconstructed ECC page from the XOR mechanism, according to reliability information (aka “soft” bits), in order to construct a page with lower BER, on which the

BCH decoder is more likely to succeed. This may be performed by utilizing the conventional XOR and BCH decoder hardware engines, as described herein.

In case a page fails BCH decoding and XOR recovery, perform the following additional steps:

- Read the failing page (denoted as P_1) from the memory.
- Generate a reconstructed version of the failing page (denoted as P_2) using the XOR mechanism: P_2 = XOR of all other pages in the XOR stripe
- Generate a soft bit page (denoted as P_{SB}), indicating which cells in the failing page are error prone (as illustrated in Figure 1).
- Generate a combined page (denoted as P_3) by combining P1 and P2 using the soft bit page P_{SB}: $P_3 = (P_1 \text{ AND } P_{SB}) \text{ OR } (P_2 \text{ AND } (\text{NOT } P_{SB}))$.
- Apply BCH decoding to the combined page P_3.

The intuition behind the proposed scheme is explained in Figure 2.

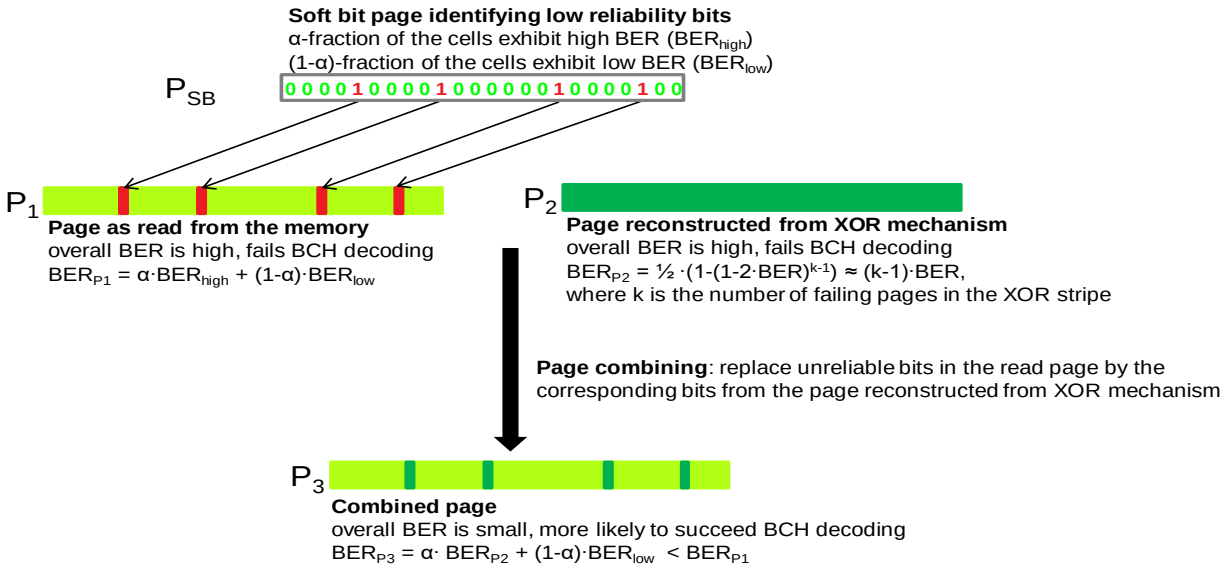


Figure 2: Leveraging the XOR overprovisioning for Soft BCH Decoding

In order to quantify the benefit of the proposed scheme, rigorous analysis of the correctable Bit Error Rate (BER) is performed. The full presentation will include the detailed theoretical analysis and simulation results. An typical graph is presented here in Figure 3.

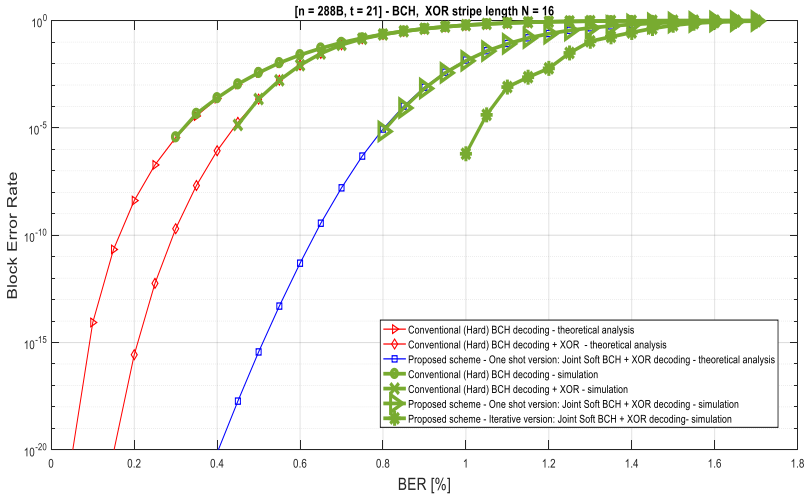


Figure 3: BLER vs. BER curves for conventional decoding and the proposed joint soft BCH&XOR decoding – theoretical and simulation results

E. Summary

Joint Soft BCH & XOR decoding scheme is proposed for SCM memories, leveraging the full allocated overprovisioning in order to boost the overall random errors correction capability by up to 4X. The scheme has low complexity and can utilize conventional XOR and BCH decoder hardware engines of SCM controllers. It can be implemented as an extra “heroics” decoding step in case the conventional BCH decoding and XOR recovery fail. It can provide significantly higher robustness to various disturb effects, extend the operational conditions ranges and improve SCM reliability, endurance and retention specs.