Resistive Memory Fully Compatible with Advanced CMOS Nodes

Jeremy Guy, Amit Prakash, Sung Hyun Jo

Crossbar Inc. 3200 Patrick Henry Dr. Suite 110, Santa Clara, CA 95054
Tel: (408) 884-0281, Fax: (408) 884-0283, Email: sung-hyun.jo@crossbar-inc.com

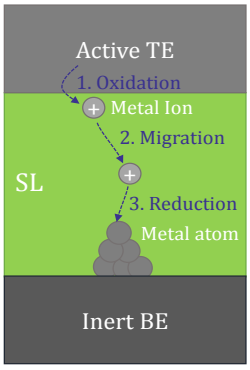
Abstract

We report the feasibility of high density Aluminum based Resistive memory (ReRAM) and its extremely good performances and behavior when coupled with optimized material stack. Sub 50nm devices integrated in 1T1R 2Mb array are offering exceptional advantages, including a Forming free switching, 400°C baking stability, outstanding 225°C retention and beyond 100k cycle endurance.

Introduction

Over the past decades, emerging Non-Volatile Memory (NVM) technologies have been widely investigated and some have already been integrated into consumer products. Along with PCM, MRAM, FeRAM etc. ReRAM belongs to these emerging NVMs, whose benefits keep growing with the increasing complexity of Flash memory scaling and integration. ReRAM offers notable advantages and qualities such as a relatively simple Metal Insulator Metal structure allowing its integration in the BEOL. ReRAM also benefits from a low voltage, low power and high speed operation, making it a natural candidate for embedded memory integration as well as neuromorphic computing, in light of the strong growth of AI and deep learning.

We present here, for the first time, an Aluminum based ReRAM with sub 50nm devices integrated in 1T1R 2Mb array offering high temperature stability, long term retention and high endurance capabilities. This technology also shows great potential to be integrated in future 1TnR structure [1].



Metal	Melting Temp (°C)
Al	660
Ag	961
Au	1064
Cu	1083
Ni	1453
Pd	1552
Ti	1660
Pt	1772
Cr	1857
Hf	2150
Ta	2996
W	3410

Fig. 1. (a) Basic Filamentary ReRAM Schematics. (b) Table of melting temperature for the metal commonly used in ReRAM

ReRAM Technology

The data storage mechanism of ReRAM is based on the modification of the electrical resistance of a Switching Layer (SL) located between two metallic electrodes (Fig. 1 a.). The resistive switching can either be filamentary, with the local formation of a conductive path in the SL; or uniform, with a global modification of SL. In our case, we will be focusing on filamentary based ReRAM and more precisely metallic filament, in opposition to oxygen vacancies filament.

To program the device (Fig. 1 a.), a positive bias is applied on the Top Electrode (TE) to oxidize it, leading to free metal ions formation and field induced diffusion through the SL. Once reaching the Bottom Electrode (BE), the ions get reduced and stabilized, progressively forming a conductive path between the two electrodes. Once the filament reaches TE, the ON state is stable. To erase the device, the process is opposite, with a positive bias applied on the BE, leading to the oxidation and dissolution of the conductive filament. With the filament dissolved, the devices is back in OFF state.

Optimized ReRAM

The first key element of the filamentary ReRAM stack is the TE, formed by an active metal, enabling oxidation and ion formation. Various metals and alloys have been investigated with the most widely known being Copper based [2] and Silver based [3] alloys. The TE acting as a metal ion's reservoir, its capacity to be oxidized is primordial to insure low voltage switching, the easier the dissolution, the lower the voltage. This capacity to be oxidized or dissolved can be correlated to the atom chemical bond strength indirectly reflected in the metal melting temperature. As can be seen in the Fig. 1 (b), Aluminum has the lowest melting point among the commonly used metals in ReRAM, making it a perfect candidate for low voltage switching.

The second key element of the ReRAM stack is the switching layer, medium of the diffusing ions. The SL is responsible, to a certain extent at least, for retention and endurance. Fig. 2 shows the excellent switching behavior of our Aluminum based ReRAM with various SL materials, from oxide to nitride. All devices are showing forming free behavior, with overlapping 1st and 2nd cycle thanks to the low oxidation energy of Aluminum. This forming free behavior is enabling the technology integration with low voltage CMOS.

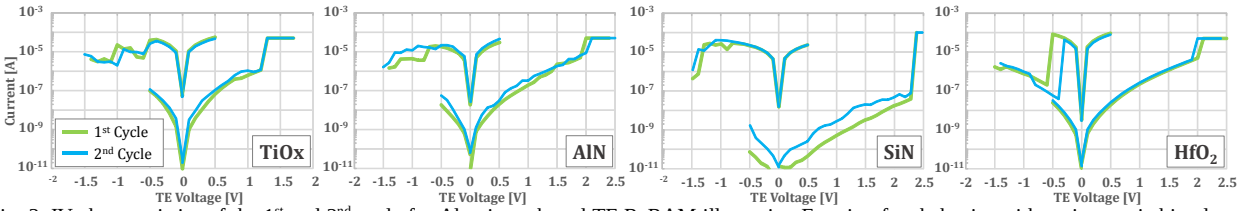


Fig. 2. IV characteristics of the 1st and 2nd cycle for Aluminum based TE ReRAM illustrating Forming free behavior with various switching layer materials

Array Integration

The previous Aluminum based TE has been coupled to an optimized SL and BE; and integrated into a 1T1R 2Mb array. Integrated devices exhibit sub 50nm dimension for improved density as well as a strong potential for further scaling below 10nm. Fig. 3 illustrates the technology scalability.

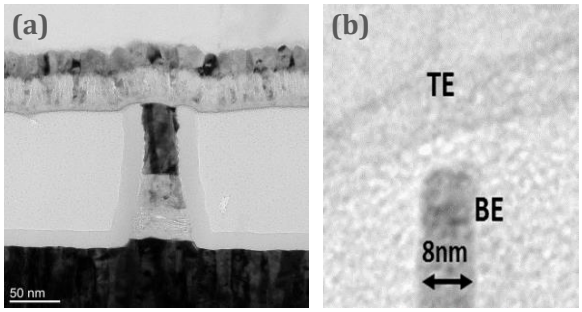


Fig. 3. (a) Sub 50nm devices integrated in 2Mb Array. (b) Sub 10nm devices proving the extreme scaling capabilities of the technology

The integrated stack relies on an optimized SL composition, enabling an extremely good high temperature stability, making the stack capable of withstanding 400°C baking, an essential step of the BEOL process. Fig. 4 shows the IV characteristic comparison before and after 400°C baking.

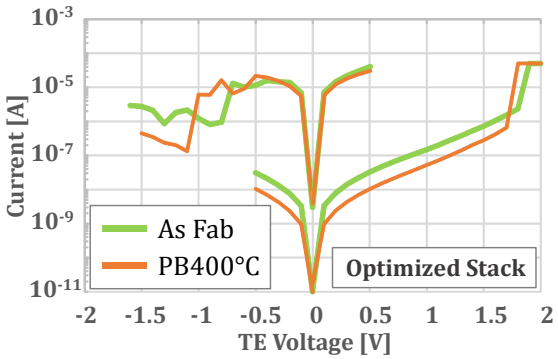


Fig. 4. IV characteristic and stability post 400°C bake, essential step to the BEOL integration

Performance wise, ON and OFF retention are extremely good at 225°C and maintained over 100k cycles endurance (Fig. 5). 260°C retention, corresponding to the soldering reflow temperature is also particularly promising right after a short optimized conditioning step (Fig. 6). Finally endurance remains on par with retention with no sign of degradation post 100k cycles (Fig. 7), a progressive increase of memory window over cycling is even observable. Overall, the technology presented here is offering very promising performances across the board.

Conclusion

For the first time Aluminum based ReRAM integrated in 1T1R 2Mb array is presented. With outstanding performances and temperature stability, this sub 50nm technology paves the way to embedded ReRAM and advanced deep learning applications.

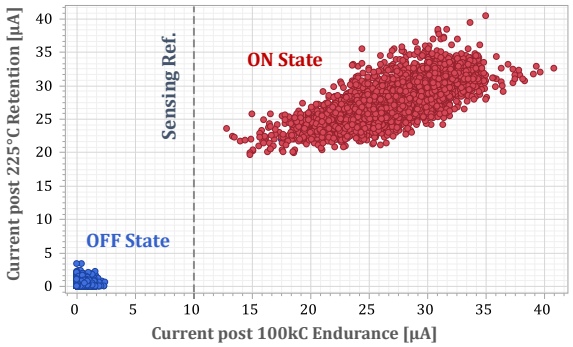


Fig. 5. Current evolution over 225°C retention bake right after 100k cycles, illustrating extremely good stability of both ON and OFF State

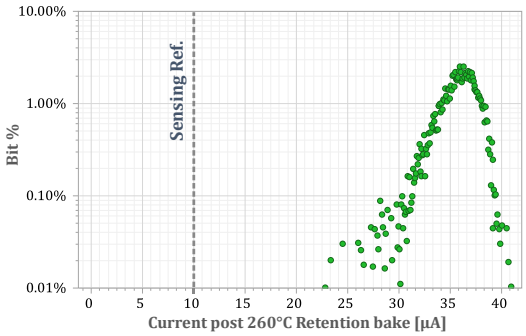


Fig. 6. Current distribution post 260°C retention bake right after short conditioning step, essential stability for the soldering reflow

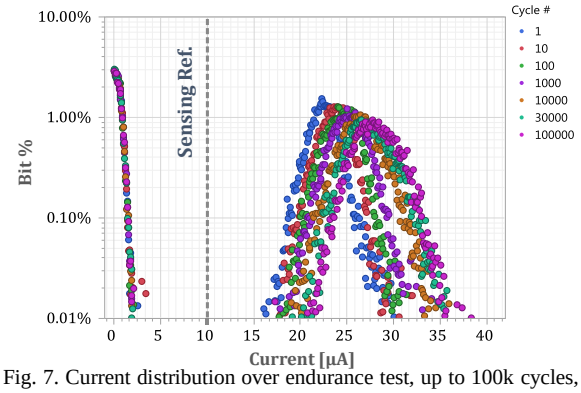


Fig. 7. Current distribution over endurance test, up to 100k cycles, illustrating memory window's stability.

References

[1] S. Jo et. al., "3D-stackable Crossbar Resistive Memory based on Field Assisted Superlinear Threshold (FAST) Selector", IEDM 2014.

[2] J. Guy et. al., "Investigation of the physical mechanisms governing data-retention in down to 10nm nano-trench Al2O3/CuTeGe conductive bridge RAM (CBRAM)", IEDM 2013.

[3] S. Jo et. al., "CMOS Compatible Nanoscale Nonvolatile Resistance Switching Memory", Nano Lett. 8, pp392-937, 2008.