March 9 – 11, 2014

UC San Diego

Hosted by:

CMRR
Center for Magnetic Recording Research

NVSL
Non-volatile Systems Laboratory
Welcome to the fifth annual UCSD Non-Volatile Memories Workshop presented by the Center for Magnetic Recording Research, and the Non-Volatile Systems Laboratory.

This workshop brings together scientists and engineers from industry and academia who are working on advanced non-volatile information storage devices and systems. The goal is to facilitate the exchange of ideas, insights, and knowledge within this broad community of practitioners and researchers, and to foster the establishment of new collaborations that can propel future progress in the design and application of non-volatile memories.

The program takes a “vertical” approach, with technical sessions that encompass solid-state and magnetic storage technologies; coding techniques for data integrity, preservation, and security; system-level storage architectures; and new applications enabled by advances in these areas
Workshop Sponsors

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Other

IEEE MAGNETICS 50 YEARS
### Non-Volatile Memories Workshop 2014

*Events and Technical Program Schedule*

#### Sunday, March 9, 2014

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<th>Time</th>
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| 1:00 pm-4:00 pm | **Tutorial Session:** Chair: Paul H. Siegel  
                       *Location: Price Center Ballroom East*  
                       Data Integrity and Reliability in Storage Stacks  
                       Microsoft Research*, Fusion-io†  
                       Cheng Huang*, Hao Zhong† |
| 6:00 pm-9:00 pm | **Reception at the Sheraton Hotel**                                    |

#### Monday, March 10, 2014

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<th>Time</th>
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<td>7:45 am-8:45 am</td>
<td><strong>Continental Breakfast at Price Center Ballroom East</strong></td>
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<td>8:45 am-9:00 am</td>
<td><strong>Opening Remarks at Price Center Ballroom East</strong></td>
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| 9:00 am-10:00 am | **Keynote Speaker:** Chair: Hemant Thapar  
                          The Flash Transformed Data Center  
                          John Scaramuzzo, SanDisk  
                          *Location: Price Center Ballroom East* |
| 10:00 am-10:45 am | **Break**                                                             |
| 10:45 am-12:05 pm | **Session I – System Architectures for Flash**  
                        Chair: Yitzhak (Tsahi) Birk  
                        *Location: Price Center Ballroom East* |
| 10:45 am-11:05 am | **High Performance Hardware-Accelerated Flash Key-Value Store**  
                          Corporate R&D Center, Toshiba Corporation*, Electrical Engineering Department,  
                          Stanford University†  
                          Shingo Tanaka*, Christos Kozyrakis† |
| 11:05 am-11:25 am | **Extending Main Memory with Flash-the Optimized SWAP Approach**  
                          Memory Solutions Lab, Memory Business, Samsung Electronics  
                          Jihyung Park, Hyuck Han, Sangyeun Cho |
| 11:25 am-11:45 am | **Controlling Program Parameters to Increase NAND Flash Life for SSD Applications**  
                          Seagate Technology  
                          Caitlin Race, Young Pil Kim, Rod Bowman |
| 11:45 am-12:05 pm | **Software-Defined Solid State Disks**  
                          UCSD  
                          Sudharsan Seshadri, Sundaram Bhaskaran, Arup De, Yanqin Jin, Robert Liu, Trevor  
                          Bunker, Steven Swanson |
<p>| 12:05 pm-1:45 pm | <strong>Lunch / Poster Session at Price Center Ballroom B</strong>                 |</p>
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<tr>
<th>Time</th>
<th>Session II – Coding for Enhanced Endurance</th>
<th>Session III - Devices</th>
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| 1:45 pm-   | Chair: Eitan Yaakobi  
*Location: Price Center Ballroom East*                                                                        | Chair: Ken Lee  
*Location: Price Center Ballroom A*                                                      |
| 3:05 pm    |                                                                                                           |                                                                                        |
| 1:45 pm-   | *Coset Coding to Extend the Lifetime of Non-Volatile Memory*                                                | *Toward High-density STT-MRAM for Embedded Memory*                                      |
| 2:05 pm    | *Duke University*  
Adam N. Jacobvitz, Robert Calderbank, Daniel J. Sorin                                                     | *LEAP*  
Toshihiro Sugii                                                                         |
| 2:05 pm-   | *Joint Rewriting and Error Correction in WOM*                                                              | *Design of Heterojunction Oxide Stack for 3D RRAM Cross-Point Array*                   |
| 2:25 pm    | *Texas A&M University*, *Texas A&M University and California Institute of Technology*, *University at Buffalo, The State University of New York*,  
Anxiao (Andrew) Jiang, Yue Li, Eyal En Gad, Michael Langberg, Jehoshua Bruck. | *Arizona State University*  
Pai-Yu Chen, Shimeng Yu                                                                    |
| 2:25 pm-   | *Write-Amplification Reduction Through Multi-Write Codes in Flash Storage*                                 | *Memory Intensive Computing*  
Technion*, *University of Rochester†*  
Shahar Kvatinsky, Eby G. Friedman†, Avinoam Kolodny*, Uri C. Weiser*                      |
| 2:45 pm    | *Compression Architecture for Bit-write Reduction in Non-volatile Memory*                                  | *Using Analog Memory with Coupled Oscillators for Pattern Recognition Applications*   |
| 3:05 pm    | *University of Pittsburgh*  
David Dgien, Nathan A. Hunter, Jiayin Li, Kartik Mohonram                                                  | *University of Pittsburgh*  
Steven P. Levitan, Donald M. Chiarulli, Yan Fang                                         |
<p>| 3:05 pm-   |                                                                                                           |                                                                                        |
| 3:25 pm    | <em>Break</em>                                                                                                   |                                                                                        |</p>
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<th>Session IV – System Architectures for Next-Generation Memories I</th>
<th>Session V – Coding for Reliability</th>
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<td>3:25 pm-</td>
<td><strong>When NVMe is too slow: low latency protocol for PCM PCIe SSDs</strong>&lt;br&gt;<strong>HGST</strong>, <strong>UCSD</strong>&lt;br&gt;Dejan Vucinic*, Qingbo Wang*, Cyril Guyot*, Robert Mateescu*, Filip Blagojevic*, Luiz Franca-Neto*, Damien Le Moal*, Trevor Bunker†, Jian Xu†, Steven Swanson†, Zvonimir Bandic*</td>
<td><strong>Low-complexity Multi-Bit Iterative Decoders for Non-Volatile Memory Channels</strong>&lt;br&gt;<strong>University of Arizona</strong>, <strong>University of Cergy-Pontoise†</strong>&lt;br&gt;Bane Vasic*, Shiva Planjery†, David Declercq†</td>
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<td>3:25 pm-</td>
<td><strong>Software Enabled Wear-Leveling for Hybrid PCM Main Memory on Embedded Systems</strong>&lt;br&gt;<strong>Oklahoma State University</strong>&lt;br&gt;Jingtong Hu</td>
<td><strong>Coding for Unreliable Memory Cells in TLC Flash</strong>&lt;br&gt;<strong>UCLA</strong>&lt;br&gt;Ryan Gabrys, Lara Dolecek</td>
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<td>4:05 pm-</td>
<td><strong>Writeback-Aware Bandwidth Partitioning for Multi-core Systems with PCM</strong>&lt;br&gt;<strong>University of Pittsburgh</strong>&lt;br&gt;Miao Zhou, Yu Du, Bruce Childers, Rami Melhem, Daniel Mosse</td>
<td><strong>Efficient Codes for Multilevel Flash Memories</strong>&lt;br&gt;<strong>Oregon State University</strong>, <strong>University of Teramo†</strong>&lt;br&gt;B. Bose*, L. Tallini†</td>
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<td>4:25 pm-</td>
<td><strong>High Endurance Low Cost Hybrid Phase-Change Memory (PCM)-NAND Flash Enterprise Class Solid-State Drives</strong>&lt;br&gt;<strong>HGST, a Western Digital company</strong>&lt;br&gt;Luiz M Franca-Neto, Robert Mateescu, Cyril Guyot, Qingbo Wang, Dejan Vucinic, Frank Chu, Zvonimir Bandic</td>
<td><strong>The Performance of Polar Codes for Multilevel Flash Memories</strong>&lt;br&gt;<strong>Texas A&amp;M and Caltech</strong>, <strong>LSI corporation†</strong>, <strong>Texas A&amp;M University‡</strong>&lt;br&gt;Yue Li*, Hakim Alhussien†, Erich F. Haratsch†, Anxiao (Andrew) Jiang‡</td>
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<td>5:00 pm-</td>
<td><strong>Shuttle bus to Sheraton hotel – for those who are not attending the dinner banquet</strong></td>
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<td>5:05 pm-</td>
<td><strong>Departure, San Diego Museum of Art</strong>, one trip only</td>
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<tr>
<td>6:30 pm-</td>
<td><strong>Dinner Banquet at San Diego Museum of Art</strong></td>
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<tr>
<td>7:45 am -</td>
<td>Breakfast at <em>Price Center Ballroom East</em></td>
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<tr>
<td>9:00 am -</td>
<td>Keynote Speaker: <strong>NVM and New Storage Design Centers</strong></td>
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<td>10:00 am</td>
<td><strong>Chair:</strong> Steven Swanson</td>
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<td>10:00 am -</td>
<td><strong>Kaladhar Voruganti, NetApp Advanced Technology Group</strong></td>
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<td>10:00 am -</td>
<td><strong>Location:</strong> <em>Price Center Ballroom East</em></td>
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<tr>
<td>10:00 am -</td>
<td><strong>Break</strong></td>
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<tr>
<td>10:45 am -</td>
<td>PARALLEL SESSIONS</td>
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<tr>
<td>10:45 am -</td>
<td><strong>Session VI - System Architectures for Next-Generation Memories II</strong></td>
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<td>10:45 am -</td>
<td><strong>Chair:</strong> Zvonimir Bandic</td>
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<td>10:45 am -</td>
<td><strong>Location:</strong> <em>Price Center Ballroom East</em></td>
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<tr>
<td>10:45 am -</td>
<td>PSS: A prototype storage subsystem based on PCM</td>
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<td>10:45 am -</td>
<td>IBM Zurich Research Lab*, University of Patras†</td>
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<td>10:45 am -</td>
<td>Ioannis Koltsidas*, Peter Mueller*, Roman Pletka*, Thomas Weigold*</td>
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<td>10:45 am -</td>
<td>Evangelos Eleftheriou*, Maria Varsamou†, Athina Ntalla†, Elina</td>
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<td>10:45 am -</td>
<td>Mpougioukou†, Aspasia Palli†, Theodoros Antonakopoulos†</td>
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<tr>
<td>11:05 am</td>
<td>Using Managed Runtimes to Tolerate Holes in Wearable Memories</td>
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<td>11:05 am</td>
<td>Australian National University*, Microsoft Research and Univ. Washington†, Microsoft Research†, EPFL◊</td>
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<td>11:05 am</td>
<td>Tiejun Gao*, Karin Strauss†, Steven Blackburn*, Kathryn McKinley‡, Doug</td>
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<td>11:05 am</td>
<td>Burger‡, James Larus◊</td>
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<td>11:05 am</td>
<td>Comparing Analytical and Simulation Models for Zombie Memories with</td>
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<td>11:25 am</td>
<td>Permanent Failure</td>
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<td>11:25 am</td>
<td>*, Microsoft Research†, University of Campinas‡</td>
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<td>11:25 am</td>
<td>John D. Davis*, Karin Strauss†, Mark Manasse†, Parikshit Gopalan†,</td>
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<td>11:25 am</td>
<td>Sergey Yekhanin†, Rodolfo Azevedo‡</td>
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<td>11:25 am</td>
<td>Introducing SSDs to the Hadoop MapReduce Framework</td>
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<td>11:25 am</td>
<td>Samsung System Architecture Lab*, Texas A&amp;M Univ.†</td>
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<td>11:25 am</td>
<td>Jaehwan Lee*, Sangwhan Moon†, Yang-Suk Kee*, Bob Brennan*</td>
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<td>11:25 am</td>
<td>LightNVM: Lightning Fast Evaluation Platform for Non-Volatile Memories</td>
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<td>11:25 am</td>
<td>IT University of Copenhagen*, Tel Aviv University†, HGST‡</td>
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<tr>
<td>11:25 am</td>
<td>Matias Bjorling*, Jesper Madsen*, Philippe Bonnet*, Aviad Zuck†, Zvonimir Bandic‡, Qingbo Wang‡</td>
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<td>11:25 am</td>
<td>High Performance Transaction Processing for NVRAM</td>
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<td>11:25 am</td>
<td>University of Michigan</td>
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<td>11:25 am</td>
<td>Steven Pelley, Thomas F. Wenisch</td>
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<tr>
<td>Time</td>
<td>Sessions</td>
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| 11:45 am-12:05 pm | Exploring Storage Class Memory with Key Value Stores  
* University of Washington  
Katelin Bailey, Peter Hornyack, Luis Ceze, Steven Gribble, Henry Levy  
Making Updates Disk I/O Friendly Using SSDs  
* IBM T.J.Watson Research Center,  
† IBM T.J.Watson Research Center,  
‡ IBM T.J.Watson Research Center  
Mohammad Sadoghi*, Kenneth Ross†, Mustafa Canim‡, Bishwaranjan Bhattacharjee* |
| 12:05 pm-1:00 pm | Lunch / Poster Session at Price Center Ballroom B |
| 1:15 pm-2:35 pm | Session VIII – Data Encoding and Mapping Techniques  
Chair: Rob Calderbank  
Location: Price Center Ballroom East |
| 1:15 pm-1:35 pm | Constrained Rank Modulation for Flash Memories  
* UCLA  
Frederic Sala, Lara Dolecek |
| 1:35 pm-1:55 pm | Codes for Fast Writes in Multi-Level NVMs  
* Technion – Israel Institute of Technology  
Evyatar Hemo, Yuval Cassuto |
| 1:55 pm-2:15 pm | Bit Mapping for Balanced PCM Cell Programming  
* University of Pittsburgh  
Yu Du, Miao Zhou, Bruce R. Childers, Daniel Mosse, Rami Melhem |
| 2:15 pm-2:35 pm | Highly Reliable Techniques for NAND Flash Memory / ReRAM Hybrid Storage  
* Chuo University / University of Tokyo,  
† Chuo University  
Shuhei Tanakamaru*, Masafumi Doi†, Ken Takeuchi† |
| 2:40 pm-3:00 pm | Break |
- Tutorial - Sunday, March 9, 2014

Tutorial
Chair: Paul H. Siegel
Price Center Ballroom East
1:00 – 4:00 PM

Data Integrity and Reliability in Storage Stacks
Cheng Huang, Hao Zhong, Microsoft Research*, Fusion-io†

Abstract: Abstract: Storage systems continue to grow rapidly in scale, both in the number of storage nodes and the capacity of individual storage components, including memory, SSDs and hard drives. As a result, data corruption and loss become more frequent throughout the storage stacks. Coping with data corruption/loss and ensuring data integrity/reliability require good understanding of error/failure characteristics and efficient, cost effective techniques. This tutorial will cover various topics on data integrity and reliability in the storage stacks, including:

- NAND Flash memory scaling trend.
- Challenges endurance and retention as NAND scaling.
- Analysis on failure mechanisms in SSD related to NAND
- Signal processing techniques for NAND flash memory
- Error correction coding for SSD
- LDPC vs. BCH
- Hard decoding vs. soft decoding
- Error and failure characteristics in memory and hard drives
- System techniques for error/failure detection and prevention
- Erasure coding across devices
- Conventional codes: RS
- Modern storage codes: LRC, PMDS/SD codes, Regenerating codes
- Case studies: Windows Azure Storage & Facebook HDFS

Bio: Cheng Huang is a researcher at Microsoft Research. He has invented technologies that have been shipped in many Microsoft products, including Windows Azure, Windows, Office, Xbox and Bing, creating commercial impact in the order of hundreds of millions of dollars. He received the best paper award at USENIX ATC in 2012 and Microsoft TCN Storage Technical Achievement award in 2013 for “outstanding achievement and contribution in storage technology.

Bio: Hao Zhong is currently senior director of NAND flash engineering at Fusion-io. He has extensive research, development and management experience on algorithms and VLSI architecture SSD controller and HDD read channel. Prior to Fusion-io, He worked for Sandforce Inc (acquired by LSI) as director of flash channel engineering where led technical collaboration with major NAND flash vendor and flash channel development. Prior to SandForce, he worked as system architect at LSI corporation.
The Flash Transformed Data Center
John Scaramuzzo
Senior VP, SanDisk Enterprise Storage Solutions

Abstract: Transformation with flash for the data center Business application users have come to expect instant access, faster responses and an increasingly better user experiences on devices. Flash has been a revolutionary enabler across consumer devices. These same benefits, user expectations and improved experiences are taking over all aspects of data storage, and driving these trends into the data center. Until now, the costs and densities of hard disk drive storage have been sufficient to delay data centers’ rapid adoption of solid state storage. While the application performance advantages for solid state storage have been widely recognized, now the industry is beginning to better understand the total cost of ownership (TCO) advantages of flash-based storage. What will soon further ramp the adoption of flash are the superior storage densities offered by solid state drives as they expand to double-digit terabyte capacities per drive, surpassing the maximum densities of hard disk drives. Lastly, vertically integrated flash storage providers will continue to drive down the cost curve for solid state memory and take on workloads in the nearline and archival tiers previously thought to be the primary domain of SATA hard disk drives. With these advantages across multiple tiers of storage, the enablement of the flash transformed data center will ultimately become a reality. Flash will eventually be a fit for every data center workload. Flash-based storage systems not only accelerate performance, they introduce agility into the overall IT equation, a must to maintain budget constraints and an integral factor in lowering overall TCO. Plus, it’s not just a matter of dollar per gigabyte any more, there are many variables – IOPS, watts, rack units and even capacity. The question becomes one of overall economics and one thing is certain: IT organizations cannot afford to ignore the shifting of the storage landscape toward flash. Join John Scaramuzzo, senior vice president and general manager of Enterprise Storage Solutions to navigate through the current state of enterprise storage, explore trends and solutions to address various storage needs, and discuss how the storage industry is uniquely positioned to enable the Flash Transformed Data Center.

Bio: John Scaramuzzo is the senior vice president and general manager of SanDisk’s Enterprise Storage Solutions team. Scaramuzzo is a veteran of the storage industry with more than 25 years of experience that includes leadership roles at Seagate, Maxtor, Quantum and Digital Equipment Corporation. Prior to joining SanDisk, he served as president of SMART Storage Systems where he was responsible for driving and expanding the company’s technology leadership and
storage business in the enterprise, OEM and channel markets, as well as in the related cloud, big data and vertical industries. Scaramuzzo holds a bachelor's degree in electrical engineering from Boston University and a master's in electrical science from Harvard University. He also holds three U.S. patents related to disk-drive technology and applications.
High Performance Hardware-Accelerated Flash Key-Value Store
Shingo Tanaka*, Christos Kozyrakis†
Corporate R&D Center, Toshiba Corporation*, Electrical Engineering Department, Stanford
University†

Abstract: Distributed in-memory key-value stores such as memcached have become a critical
caching layer for low latency Web 2.0 systems. We present high performance key-value store
that uses hardware acceleration in FPGA and utilizes both DRAM cache and Flash memory to
achieve both high storage capacity and high query throughput. Our system achieves up to 20M
qps which is more than 10x higher than software memcached and 1.5x higher than the best
published hardware design, having only 3.8us latency.

Bio: Shingo Tanaka is a Senior Research Scientist in Corporate Research &
Development Center at Toshiba Corporation. He received the M.E. degree in
Mechanical Engineering from the University of Tokyo in 2001. His current
research interests are high performance and energy efficient storage
networking and computer architecture for large scale systems. He is currently
working on hardware acceleration technology on network and database
processing that utilizes flash memory advantages.

Extending Main Memory with Flash-the Optimized SWAP Approach
Jihyung Park, Hyuck Han, Sangyeun Cho
Memory Solutions Lab, Memory Business, Samsung Electronics

Abstract: Various approaches to memory-efficient data processing now face the limitation of
DRAM capacity with continuously increasing data footprints. In this talk, we present virtual
memory extension with flash memory to effectively elide the DRAM cost and capacity issues.

Bio: Jihyung Park is a Senior Engineer in the Memory Solutions Lab at the
Samsung Memory Business. He has worked for the Samsung Storage Business as
a software developer. His research interests include Operating System, Device
Firmware, Key-Value Storage and (In-Memory) Database Systems.
Controlling Program Parameters to Increase NAND Flash Life for SSD Applications
Caitlin Race, Young Pil Kim, Rod Bowman
Seagate Technology

Abstract: Performance gains from scaling NAND flash memory have come at the expense of data retention and reliability, both of which get worse with time and media use. Standard techniques to overcome these issues include garbage collection and overprovisioning. This paper introduces another method to improve the reliability of NAND by changing the program verify voltage over the lifetime of the flash so as to minimize damage, especially in early life where there is more ECC power than required.

Bio: Young Pil Kim received M.S. and Ph.D. degrees in Physics and Materials Science and Engineering in 1992 and 1998, respectively, from Korea Advanced Institute of Science and Technology (KAIST), and worked for major semiconductor memory manufacturers, Samsung, Micron, and IM Flash Technologies, for more than 15 years on DRAM and NAND Flash process integration, cell transistor development, process/device reliabilities, and root-cause failure analysis. He had actively contributed to international conferences and served as technical program committees and sub-committees for IRPS and VLSI-TSA in 2009 and 2001, respectively. He currently works for Seagate Technology in Solid State Drive (SSD) Media Technology focusing on NAND/emerging media characterization, reliability evaluation, and failure analysis in developing SSD and Solid State Hybrid Drive (SSHD).

Software-Defined Solid State Disks
Sudharsan Seshadri, Sundaram Bhaskaran, Arup De, Yanqin Jin, Robert Liu, Trevor Bunker, Steven Swanson
UCSD

Abstract: We explore the potential of making programmability a central feature of the SSD interface. Our prototype system, called the Easily Programmable SSD (EPSSD), allows programmers to augment and extend the semantics of an SSD with application specific features. The SSD Apps running on the EPSSD give application logic low-latency, high-bandwidth access to the SSD’s contents while reducing the load that IO processing places on the host processor. The programming model for SSD Apps provides great flexibility, supports the concurrent execution of multiple SSD Apps in the EPSSD, and supports the execution of trusted code in the EPSSD.

Our prototype implementation demonstrates the effectiveness and flexibility of the EPSSD by implementing five SSD Apps and comparing their complexity and performance to fixed-function implementations. We find that defining SSD semantics in software drastically reduces the time required to implement new functions while reducing performance by just a small
margin. As a result, the EPSSD makes it feasible for almost any application developer to benefit from a customized SSD interface.

**Bio:** Steven Swanson is an associate professor in the Department of Computer Science and Engineering at the University of California, San Diego and the director of the Non-volatile Systems Laboratory. His research interests include the systems, architecture, security, and reliability issues surrounding non-volatile, solid-state memories. He also co-leads projects to develop low-power co-processors for irregular, mobile applications (e.g., Android Apps) and to devise software techniques for using multiple processors to speed up single-threaded computations. In previous lives he has also worked on scalable dataflow architectures, ubiquitous computing, and simultaneous multithreading. He received his PhD from the University of Washington in 2006.
Parallel Sessions

Session II – Coding for Enhanced Endurance 1:45 PM – 3:05 PM
Chair: Eitan Yaakobi
Price Center Ballroom East

Coset Coding to Extend the Lifetime of Non-Volatile Memory
Adam N. Jacobvitz, Robert Calderbank, Daniel J. Sorin
Duke University

Abstract: PCM and Flash memory cells both wear out based on usage. PCM is limited in the number of writes it can sustain, and Flash in the number of Program/Erase cycles. In this talk we present a technique based on coset coding that can be used to increase the effective lifetime of non-volatile memories. We will also discuss our implementation of coset coding in a prototype Flash-based SSD.

Bio: Adam Jacobvitz is a 5th year Ph.D student at Duke University. He is advised by Prof. Daniel Sorin and collaborates with Prof. Robert Calderbank. His research interests lie at the intersection of computer architecture and coding theory. His research efforts focus on improving the lifetime characteristics of non-volatile memory technologies.

Joint Rewriting and Error Correction in WOM
Anxiao (Andrew) Jiang*, Yue Li†, Eyal En Gad‡, Michael Langberg◊, Jehoshua Bruck‡
Texas A&M University*, Texas A&M University and California Institute of Technology†,
California Institute of Technology‡, University at Buffalo, The State University of New York◊

Abstract: Both rewriting and error correction are important technologies for non-volatile memories, especially flash memories. However, coding schemes that combine them have been limited. This paper presents a new coding scheme that combines rewriting and error correction for the write-once memory model. Its construction is based on polar codes, and it supports any number of rewrites and corrects a substantial number of errors. The code is analyzed for the binary symmetric channel, and experimental results verify its performance. The results can be extended to multi-level cells and more general noise models.

Bio: Eyal En Gad received the B.Sc. degree in 2008 from the Electrical Engineering Department, Technion—Israel Institute of Technology, Haifa, Israel. He is now a doctoral student with the Department of Electrical Engineering, of Pittsburgh. His research interests investigate the use of emerging non-volatile memory technologies for use as main memory in high performance computing systems. California Institute of Technology, Pasadena. His research interests include information and coding theory with data storage applications.
Write-Amplification Reduction Through Multi-Write Codes in Flash Storage
Saher Odeh, Yuval Cassuto
Technion – Israel Institute of Technology

Abstract: In this work we investigate how to cleverly employ multi-write codes within the flash translation layer (FTL). The two proposed architectures combine between standard access and re-write access and exploit the workload locality to reduce the write-amplification significantly. These architectures show clear advantage over no re-write and known re-write schemes for both synthetic workloads and industry-accepted benchmark traces. Joint work with Saher Odeh.

Bio: Yuval Cassuto is a faculty member and a Viterbi computer-engineering fellow at the Department of Electrical Engineering of the Technion – Israel Institute of Technology. His research interests include coding theory, coding techniques for data storage, memory and storage architectures+algorithms, and data distribution in networks. His work on coding for flash memories has won the IEEE Communications Society’s 2010 best student paper award in data storage.

Compression Architecture for Bit-write Reduction in Non-volatile Memory Technologies
David Dgien, Nathan A. Hunter, Jiayin Li, Kartik Mohonram
University of Pittsburgh

Abstract: This paper describes a compression-based architecture for bit-write reduction in emerging non-volatile memories (NVMs). Bit-write reduction has many practical benefits, including lower write latency, lower dynamic energy, and enhanced endurance. The proposed architecture, which is integrated into the memory controller, relies on (i) a frequent pattern compression engine, (ii) a comparator to reduce bit-writes, and (iii) an opportunistic wear leveler to spread writes and enhance memory endurance by reducing the peak bit-writes/cell. Trace-based simulations of the SPEC CPU2006 benchmarks show a 20X reduction in raw bit-writes, which corresponds to a 2-3X improvement over the best state-of-the-art methods, and a 20% reduction in peak cell bit-writes, improving NVM lifetime.

Bio: David Dgien is a graduate student in electrical and computer engineering at the University of Pittsburgh. His research interests investigate the use of emerging non-volatile memory technologies for use as main memory in high performance computing systems.
Toward High-density STT-MRAM for Embedded Memory

Toshihiro Sugii
LEAP

Abstract: We report the current status of our spin-transfer torque magnetic RAM (STT-MRAM) development from the point of memory density for embedded memory. Toward high density STT-MRAM, we have two scenarios. One scenario is to realize small MTJ with enough fabrication margin. Another one is to realize effective high density memory by using a multi level cell (MLC). We fabricated STT-MRAMs according to two scenarios and realized small MRAM cells.

Bio: Toshihiro Sugii received the B.S., M.S., and Ph.D. degree in electrical engineering from Tokyo Institute of Technology in 1979, 1981, and 1991. In 1981, he joined Fujitsu Laboratories Ltd., Japan, where he engaged in development of CMOS devices. Since 2010, he has joined Low-power Electronics Association & Project (LEAP), Japan, where he is directing the national project on STT-MRAM. Dr. Sugii is a fellow of the Japan Society of Applied Physics and a member of the IEEE electron device society.

Design of Heterojunction Oxide Stack for 3D RRAM Cross-Point Array

Pai-Yu Chen, Shimeng Yu
Arizona State University

Abstract: Resistive switching random access memory (RRAM) is one of the most promising candidates for the next-generation non-volatile memory. To enable large capacity RRAM array, the 3D architecture is needed. A 3-layer thin film heterojunction oxide stack is proposed for RRAM to suppress the sneak current for the half-selected cell during the write operation. The I-V characteristics of the heterojunction are verified by the trap-assisted tunneling (TAT) model.

Bio: Pai-yu Chen received his B.S. in Electrical engineering from National Taiwan University in 2010 and his M.S.E. in Solid-state electronics from The University of Texas at Austin in 2013. He is now working on his Ph.D. in Arizona State University and his research interest involves emerging memory device and architecture design and new computing paradigm exploration.
Memory Intensive Computing
Shahar Kvhatinsky*, Eby G. Friedman†, Avinoam Kolodny*, Uri C. Weiser*
Technion*, University of Rochester†

Abstract: Over the past years, new memory technologies such as RRAM, STT-MRAM, and PCM have emerged. These technologies employ devices located within the metal layers of the chip, which are relatively fast, dense, and power efficient and can be considered as 'memristors'. To date, research in these devices has primarily focused on memristors as flash, DRAM, and SRAM replacement. In this presentation, we present these emerging memory technologies as enablers to the era of memory-intensive computing, which brings interesting opportunities for novel architectural applications. As an example, we present the multistate pipeline register (MPR), a structure that stores the microarchitectural state of multiple threads. We show that MPR can eliminate the need to flush the pipeline upon a thread switch in Switch-on-Event (SoE) multi-threading machines. We call the new microarchitectural scheme, Continuous Flow Multi-Threading (CFMT), and compare the performance and power consumption against traditional SoE machines. Memristor-based CFMT exhibits an average performance improvement of 40%, while reducing power consumption by 6.5%, significantly increasing the performance to energy ratio.

Bio: Shahar Kvatinsky is a Ph.D. candidate at the electrical engineering department at the Technion – Israel Institute of Technology. He received his B.Sc. in computer engineering and applied physics, and an MBA at 2009 and 2010, respectively, both from the Hebrew University of Jerusalem. Prior to his Ph.D. studies he worked for Intel as a circuit designer.

Using Analog Memory with Coupled Oscillators for Pattern Recognition Applications
Steven P. Levitan, Donald M. Chiarulli, Yan Fang
University of Pittsburgh

Abstract: We explore the use of coupled oscillators, rather than Boolean logic, which provides for implementations using emerging nano-technology that has the potential of lower energy and higher density than CMOS for associative memory. However, these systems require digital storage and per-word D/A conversion for parallel operation. Non-volatile, low-power, analog memory integrated with the oscillator technology could maintain the power, speed and area advantages of these oscillator based architectures.

Bio: Steven P. Levitan is the John A. Jurenko Professor of Computer Engineering in the Department of Electrical and Computer Engineering at the University of Pittsburgh. He received his M.S. and Ph.D. in Computer Science from the University of Massachusetts, Amherst. He is Past Chair of the ACM Special Interest Group on Design Automation (SIGDA). He was General Chair of the 44th ACM/IEEE Design Automation Conference in 2007. His research interests include
parallel and non-Boolean computing systems.

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**When NVMe is too slow: low latency protocol for PCM PCIe SSDs**

Dejan Vucinic*, Qingbo Wang*, Cyril Guyot*, Robert Mateescu*, Filip Blagojevic*, Luiz Franca-Neto*, Damien Le Moal*, Trevor Bunker†, Jian Xu†, Steven Swanson†, Zvonimir Bandic*

* HGST, † UCSD

**Abstract:** We present a new, minimalist interface protocol that allows 700000 small random reads per second at queue depth one from a PCI Express storage device.

**Bio:** Dejan Vucinic earned a Ph.D. in experimental particle physics from MIT in 1998. After a career building instruments for brain imaging, he is now at HGST, a Western Digital company, focusing on finding better ways to store and retrieve humanity’s memories.

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**Software Enabled Wear-Leveling for Hybrid PCM Main Memory on Embedded Systems**

Jingtong Hu

Oklahoma State University

**Abstract:** Phase Change Memory is a promising DRAM replacement in embedded systems due to its attractive characteristics. However, relatively low endurance has limited its practical applications. In this paper, we propose software enabled wear-leveling techniques to further extend PCM’s lifetime when it is adopted in embedded systems. A polynomial-time algorithm, the Software Wear-Leveling (SWL) algorithm, is proposed in this paper to achieve wear-leveling without hardware overhead.

**Bio:** Dr. Jingtong Hu received his B.E. degree from School of Computer Science and Technology, Shandong University, China in 2007 and M.S. and Ph.D. degree in Computer Science from the University of Texas at Dallas, in June 2010 and Aug. 2013, respectively. He is now an Assistant Professor in the School of Electrical and Computer Engineering at Oklahoma State University. His research interests include high performance and low power embedded systems, wireless sensor network, and non-volatile memory.
Writeback-Aware Bandwidth Partitioning for Multi-core Systems with PCM
Miao Zhou, Yu Du, Bruce Childers, Rami Melhem, Daniel Mosse
University of Pittsburgh

Abstract: This paper uses a writeback-aware analytic model to derive the bandwidth allocation strategy that is suitable for hybrid memory architecture comprised of a large PCM and a small DRAM. From the derivation of the model, WBP is proposed to partition PCM service cycles among applications. WBP uses a partitioning weight to indicate the importance of writebacks. A companion DWA scheme dynamically selects the partitioning weight to maximize system performance.

Bio: Miao Zhou received the B.S. and M.S. degrees in Computer Science from Huazhong University of Science and Technology in 2004 and 2007, respectively. He has been a Ph.D. student at the Computer Science department, University of Pittsburgh since 2008. His current research interests include architecture design of energy efficient memory systems related to phase change memory.

High Endurance Low Cost Hybrid Phase-Change Memory (PCM)-NAND Flash Enterprise Class Solid-State Drives
Luiz M Franca-Neto, Robert Mateescu, Cyril Guyot, Qingbo Wang, Dejan Vucinic, Frank Chu, Zvonimir Bandic
HGST, a Western Digital company

Abstract: At 20nm, MLC NAND Flash has produced parts with endurance below 5,000 write/erase cycles. TLC NAND (3 bits/cell) provides higher density at still lower endurances of < 1,000 write cycles. In this work, we show how the skew in enterprise write workload can be exploited and commercial Phase-Change Memory (PCM) parts can be added to TLC NAND Flash parts to make enterprise class hybrid SSDs 20x higher endurance than a 100% MLC-based SSD at 76% of the cost.

Bio: Luiz M Franca-Neto is a Technical Lead/Research Staff Member (RSM) at the San Jose Research Center (SJRC) of HGST, a Western Digital company. He has 40+ already granted US PTO patents and research results published in peer-reviewed international conference proceedings, invited talks, and periodicals. Luiz earned his Ph.D. in Electrical Engineering from Stanford University, USA, in 1999. (http://www.linkedin.com/pub/luiz-m-franca-neto/0/b48/671)
Low-complexity Multi-Bit Iterative Decoders for Non-Volatile Memory Channels

Bane Vasic*, Shiva Planjery†, David Declercq†

University of Arizona *, University of Cergy-Pontoise†

Abstract: We present a new type of iterative decoders for low-density parity check (LDPC) codes that use simple Boolean functions for variable node processing and surpass the belief propagation decoders in the error floor region. We discuss the error-rate performance, guaranteed error correction capability, hardware architecture, and implementation complexity of these decoders. We will present results with code and decoder parameters suitable for application in non-volatile memories.

Bio: Shiva received a Ph.D. in Electrical Engineering from the University of Arizona in Aug. 2013, and from the University of Cergy-Pontoise, France in Dec. 2012, under a dual doctoral program. His research focused on the design and analysis of low-complexity finite-precision LDPC decoders. He is currently the CEO of Codelucida LLC, a startup based in Tucson, AZ co-founded with his former Ph.D. advisors Bane Vasic and David Declercq, that develops new customized LDPC solutions for SSDs and HDDs.

Coding for Unreliable Memory Cells in TLC Flash

Ryan Gabrys, Lara Dolecek

UCLA

Abstract: In this work, we extend the model introduced by Gabrys et al. [1] to account for the presence of unreliable memory cells. Leveraging data analysis from a TLC Flash memory device, we show that memory cells within the Flash device can be broadly categorized into reliable and unreliable cells where the unreliable cells are much more likely to err than the reliable ones. Our approach will be to still program using these unreliable cells but in a limited capacity.

Bio: Ryan Gabrys received his B.S. in Computer Science from the University of Illinois, Champaign-Urbana in 2005. He was awarded the SMART scholarship in 2010 and since then has been pursuing a PhD at UCLA under the supervision of Professor Lara Dolecek. His research interests include coding schemes with applications to new storage systems and synchronization channels.
Efficient Codes for Multilevel Flash Memories
B. Bose*, L. Tallini†
Oregon State University*, University of Teramo†

Abstract: This paper contains some simple code constructions to control errors measured under the $L_{1}$ distance. Such codes find direct application in multilevel flash memory design. Some efficient asymmetric $L_1$ distance codes and symmetric $L_1$ distance codes are described. Their encoding and decoding algorithms are also explained.

Bio: Bella Bose has been at Oregon State University since 1980 and has been the Associate Director for the School of Electrical Engineering and Computer Science since 2003. He works in the areas of error correcting codes, parallel processing and computer networks. He is a Fellow of both Institute of Electrical and Electronic Engineering (IEEE) and Association for Computing Machinery (ACM).

The Performance of Polar Codes for Multi-level Flash Memories
Yue Li*, Hakim Alhussien†, Erich F. Haratsch†, Anxiao (Andrew) Jiang‡
Texas A&M and Caltech*, LSI corporation†, Texas A&M University‡

Abstract: This paper addresses several challenges raised when using polar codes in MLC flash. We propose efficient schemes for shortening polar codes, making its codewords be easily adapted to a flash page of any size. The performance of shortened polar codes is comparable to LDPC codes on the data obtained from flash. We show the feasibility of an adaptive decoding framework that does not need repeatedly code construction. Experimental results suggest its performance approach the optimized performance.

Bio: Yue is a Ph.D student at Texas A&M University, and a visiting graduate student at Caltech. His advisors are Prof. Andrew Jiang and Prof. Shuki Bruck. His research focuses on both theoretical and practical aspects of coding techniques for emerging memory systems such as flash memories and phase-change memories. Yue received his BS in information security from Huazhong University of Science and Technology in 2008, and worked as a research intern in the Flash Components Division at LSI in 2013.
NVM and New Storage Design Centers
Kaladhar Voruganti
Senior Technical Director, NetApp Advanced Technology Group

Abstract: Historically, the network storage design center has tried to simultaneously address the needs of both performance sensitive (IOPs) and idle (capacity) data. In this talk we analyze how this traditional storage design center is being challenged by new emerging design centers in order to handle the needs of latency sensitive applications at better cost points. Specifically we will discuss 1) the needs of latency sensitive real-time analytics applications (e.g. real-time stock trading, gaming, mobile ad placement, real-time supply chain management) 2) discuss how NVM is influencing how applications are being re-architected to access persistent storage (e.g. new APIs, data structures) and 3) discuss how NVM is influencing new types of storage architectures (e.g. NVM at host, pure NVM arrays, hybrid network storage controllers, hybrid disks).

Bio: Kaladhar Voruganti is currently a Senior Technical Director in the CTO office at NetApp. He provides 1) technical direction to around 60 researchers in his group 2) is driving the management by “Service Level Objective” (SLO) initiative across the company and 3) is responsible for driving the “Analysis of New Technology Trends” work across the company. Previously, he worked as a Research Staff Member at IBM Almaden Research Center, in San Jose. He got both his PhD in Computing Science and BSc in Computer Engineering from University of Alberta, in Edmonton, Canada.
Parallel Sessions

Session VI – System Architectures for Next-Generation Memories II
Chair: Zvonimir Bandic
Price Center Ballroom East

10:45 AM – 12:05 PM

PSS: A prototype storage subsystem based on PCM
Ioannis Koltsidas*, Peter Mueller*, Roman Pletka*, Thomas Weigold*, Evangelos Eleftheriou*, Maria Varsamou†, Athina Ntalla†, Elina Mpougioukou†, Aspasia Palli†, Theodoros Antonakopoulos†
IBM Zurich Research Lab*, University of Patras†

Abstract: Phase-Change Memory is emerging as one of the most promising NVM technologies with cost and performance characteristics in between those of DRAM and Flash. In this presentation we describe the design and implementation of PSS, a PCM-based Storage Subsystem which is connected to the host over the PCI-e bus. We present the hardware architecture of the card, as well as certain aspects of the firmware and the host driver. A detailed experimental evaluation of the card demonstrates the feasibility of PCM-based storage devices exhibiting performance, endurance and reliability characteristics suitable for enterprise storage.

Bio: Ioannis Koltsidas is a Research Staff Member at the IBM Zurich Research Lab. He received a B.S. degree in Electrical and Computer Engineering from the National Technical University of Athens, Greece and a Ph.D. degree in Computer Science from the University of Edinburgh, UK. He subsequently joined IBM at the Zurich Research Lab, where he has worked on Flash-based storage, tape storage and distributed file systems.

Using Managed Runtimes to Tolerate Holes in Wearable Memories
Tiejun Gao*, Karin Strauss†, Steven Blackburn*, Kathryn McKinley‡, Doug Burger‡, James Larus◊
Australian National University*, Microsoft Research and Univ. Washington†, Microsoft Research‡, EPFL◊

Abstract: Wearable main memory can benefit from system support to handle premature permanent failures. The proposed approach hides such failures from applications by using the memory abstraction offered by managed languages. Once a memory line can no longer be corrected, rather than discarding an entire page, the hardware communicates the failed line to a failure-aware OS and runtime. The runtime ensures memory allocations never use failed lines and moves data when lines fail during program execution.
Bio: Karin Strauss is a researcher at Microsoft Research and an affiliate faculty member at the University of Washington. Her research interests include computer architecture, mobile and cloud systems, and living systems in-cell computation. She has been working on addressing future challenges of memory, with focus on wear and power issues. She is an IEEE and ACM Senior Member.

Comparing Analytical and Simulation Models for Zombie Memories with Permanent Failure
John D. Davis*, Karin Strauss†, Mark Manasse†, Parikshit Gopalan†, Sergey Yekhanin†, Rodolfo Azevedo‡
* Microsoft Research†, University of Campinas‡

Abstract: We describe the Zombie framework, first introduced at ISCA 2013 [3], and then present new material: a comparison between using an analytical model and simulation to estimate the benefits of Zombie. Zombie is an endurance management framework that enables a variety of error correction mechanisms to extend the lifetimes of memories that suffer from bit failures caused by wearout, such as phase-change memory (PCM). Zombie supports both single and multi-level cell variants.

Bio: This work was done while John D. Davis was at Microsoft Research in Silicon Valley. His research interests include computer architecture, non-volatile memories, memory and storage systems, data center design, efficiency and power modeling, and low power processor design.

Exploring Storage Class Memory with Key Value Stores
Katelin Bailey, Peter Hornyack, Luis Ceze, Steven Gribble, Henry Levy
University of Washington

Abstract: We present Echo, a persistent key-value storage system designed to leverage the advantages and address the challenges of SCM. Echo achieves its scalability and recoverability for a range of data granularities through the use of a two-level memory design targeted for memory systems containing both DRAM and SCM, exploitation of SCM’s byte addressability for fine-grained transactions in nonvolatile memory, and the use of snapshot isolation for concurrency, consistency, and versioning.

Bio: Katelin Bailey is a graduate student with the systems and architecture group at the University of Washington. Her research interests address the impact of emerging non-volatile memory technologies on operating systems: from the storage system to the process model.
Introducing SSDs to the Hadoop MapReduce Framework
Jaehwan Lee*, Sangwhan Moon†, Yang-Suk Kee*, Bob Brennan*
Samsung System Architecture Lab*, Texas A&M Univ.†

Abstract: This presentation compares SSD performance to HDD performance within a Hadoop MapReduce framework. It identifies extensible best practices that can exploit SSD benefits within Hadoop frameworks when combined with high network bandwidth and increased parallel storage access. Terasort benchmark results demonstrate that SSDs presently deliver significant costeffectiveness when they store intermediate Hadoop data, leaving HDDs to store Hadoop Distributed File System (HDFS) source data.

Bio: Jaehwan Lee is a research scientist for Samsung System Architecture Lab in Bay area. His research interests include cloud computing infrastructure and big data application using flash/NVM technology. He received his Ph.D. in computer science from the University of Maryland, College Park, and his M.S. and B.S. from Seoul National University. He worked for Korea Telecom for five years as a senior researcher before his Ph.D. study.

LightNVM: Lightning Fast Evaluation Platform for Non-Volatile Memories
Matias Bjørling*, Jesper Madsen*, Philippe Bonnet*, Aviad Zuck†, Zvonimir Bandic‡, Qingbo Wang‡
IT University of Copenhagen*, Tel Aviv University†, HGST‡

Abstract: We present LightNVM, an SSD evaluation platform, that is both magnitude faster of current solutions, but also presents a highly scalable engine for low-latency memory designs, such as PCM and MRAM, to evaluate novel research work, without using an expensive evaluation platform.

Bio: Matias Bjørling is a Ph.D student at IT University of Copenhagen, Denmark. Previous works include performance characterization of NAND-flash based SSDs, cross-layer optimizations in regard to operating systems and database systems using non-volatile storage, and a multi-queue block layer for the Linux kernel.
High Performance Transaction Processing for NVRAM
Steven Pelley, Thomas F. Wenisch
University of Michigan

Abstract: Software must evolve to minimize execution overheads and reduce delays related to NVRAM writes while ensuring correct recovery. To demonstrate this concept we outline new software designs for online transaction processing (OLTP) using NVRAM, originally published in VLDB. We then argue, based on our experience designing database software, for NVRAM memory architectures and interfaces to minimize persist delays and ease programming.

Bio: Steven Pelley recently earned his Ph.D. from the University of Michigan in Computer Science and Engineering where his research interests included emerging storage technologies and database applications for such devices. He will be joining Snowflake Computing in San Mateo, California.

Making Updates DiskI/O Friendly Using SSDs
Mohammad Sadoghi*, Kenneth Ross†, Mustafa Canim‡, Bishwaranjan Bhattacharjee*
IBM T.J.Watson Research Center*, IBM.T.J.Watson Research Center†, IBM. T.J.Watson Research Center‡

Abstract: Multiversion databases store both current and historical data. We develop novel techniques for reducing index maintenance in multiversion databases, so that indexes can be used effectively for analytical queries over the current data without being a burden on transaction throughput. We re-design persistent index structures within the storage hierarchy to employ an extra level of indirection stored on SSDs, so that traversing the extra level of indirection incurs a relatively small overhead.

Bio: Mohammad Sadoghi is a Research Staff Member at IBM T.J. Watson. His research interests include designing high-performance analytical and transactional systems that exploit modern hardware advances (e.g., multi-cores, non-volatile memory, and FPGA/GPU). He is also interested in uncertainty and inconsistency that arise in integrating heterogeneous data sources on the web. He received his BSc, MSc, PhD in Computer Science from the University of Toronto.
Constrained Rank Modulation for Flash Memories
Frederic Sala, Lara Dolecek
UCLA

Abstract: Rank modulation schemes for Flash represent information by the relative rankings of cell charge levels. This approach has many benefits, but is still affected by a common Flash problem: inter-cell coupling, which results in inadvertently increasing the charge level of adjacent cells. We propose permutation constraints to mitigate the impact of inter-cell coupling while using rank modulation. We study a particular permutation constraint and resulting code rates, capacities, and other properties.

Bio: Frederic Sala is a third-year Ph.D. student in the Department of Electrical Engineering at UCLA, working with Prof. Lara Dolecek. He received his B.S.E. degree in Electrical Engineering from the University of Michigan, Ann Arbor, in 2010. His research interests are in the area of communications and information theory with a focus on channel coding, including application to synchronization channels and non-volatile memories.

Codes for Fast Writes in Multi-Level NVMs
Evyatar Hemo, Yuval Cassuto
Technion – Israel Institute of Technology

Abstract: Multi level cells (MLC) are used in non-volatile memories in order to increase storage density. Using multi-level cells, however, imposes higher read and write latencies limiting high speed applications. In this work we study the tradeoff between storage density and read/write speed in the context of providing access-speed heterogeneity within the same memory media. The main tool for that are codes that give high read and write speeds for a given redundancy budget. Joint work with Evyatar Hemo.

Bio: Yuval Cassuto is a faculty member and a Viterbi computer-engineering fellow at the Department of Electrical Engineering of the Technion – Israel Institute of Technology. His research interests include coding theory, coding techniques for data storage, memory and storage architectures-algorithms, and data distribution in networks. His work on coding for flash memories has won the IEEE Communications Society’s 2010 best student paper award in data storage.
Bit Mapping for Balanced PCM Cell Programming
Yu Du, Miao Zhou, Bruce R. Childers, Daniel Mosse, Rami Melhem
University of Pittsburgh

Abstract: Write bandwidth is an inherent performance bottleneck for Phase Change Memory (PCM) for two reasons. We observed that an unbalanced distribution of modified data bits among cell groups significantly increases PCM write time and hurts effective write bandwidth. We propose double XOR mapping (D-XOR) to distribute modified data bits among cell groups in a balanced way. Our techniques lead to a 51% average reduction in write service time for a PCM main memory with ECC, which increases IPC by 12%.

Bio: Yu Du is pursuing a PhD in Computer Science at the University of Pittsburgh. His research interests include 3D-stacked cache/memory, large-capacity hybrid memory systems. Du has a MS Shanghai Jiaotong University in 2004, and a BS from Shanghai Jiaotong University, in 2001.

Highly Reliable Techniques for NAND Flash Memory / ReRAM Hybrid Storage
Shuhei Tanakamaru*, Masafumi Doi†, Ken Takeuchi†
Chuo University / University of Tokyo*, Chuo University†

Abstract: 4 highly reliable techniques are introduced for NAND flash memory / ReRAM hybrid storage: reverse-mirroring (RM), error-reduction synthesis (ERS), page-RAID, and error-masking (EM). RM improves BER by 69% by re-ordering the write data. ERS corrects error based on the error characteristics for 91% BER reduction. Page-RAID improves acceptable BER by 45% with block parity and EM eliminates 67% bit-errors with error-location table. In summary, the acceptable BER improves by 32-times.

Bio: Shuhei Tanakamaru received the B.E. and M.E. degrees in engineering in 2009 and 2011 from the University of Tokyo, Tokyo, Japan, where he is currently working toward the Ph.D. degree. He has been engaged in a research on low power DRAM, SRAM and highly reliable solid-state drive (SSD).
#2 - Non-Volatile Memory Based Cache Replacement Policy
Presenter:

#4 - Combining the Phoenix Flash Code with the Binary Index Flash Code for Low Write Deficiency
Presenter:

#10 - Extending endurance of Phase Change Memories
Presenter:

#16 - Improving SSD Reliability with RAID via Elastic Striping and Anywhere Parity
Presenter:

#17 - Linux Memory-Mapped I/O Performance with Fast Block Devices and Multi-Queue Drivers
Presenter:

#20 - A High Performance and High Scalability File System Design for Non-Volatile Main Memory
Presenter:

24 Improving the Performance and Endurance of Mobile Flash Storage by Eliminating Double-Write Induced Redundant Writes
Presenter:

25 Reed-Solomon Codes for Die-Kill Protection in SSDs
Presenter:

27 OWBP: Offline Write Buffer Policy for Flash-Aware Storage and Memory Systems
Presenter:

29 Eliminating the Performance Cost of Data Durability: An In-Memory Database Systems (IMDS) Using NVDIMM as Storage
Presenter:

33 Analysis of Data Randomization of NAND flash Solid-State Drive Media
Presenter:
InDiE: In-Disk Evaluator for MySQL
Presenter:

Error-correction for rewriting in noisy phase-change memories
Presenter:

Optimality of Polar codes for the endurance of phase-change memories
Presenter:

Introducing Intra-SSD Duplication to Reduce Latency Variance
Presenter:

Algebraic Coding for Codes Based on Rank Modulation
Presenter:

Write-Once-Memory-Code Phase Change Memory
Presenter:

On the Existence Proof and Constructs of Random Input-Output Codes for Faster Random Read Performance of NAND Flash Memory
Presenter:

Optimizing Checkpoints Using NVM as Virtual Memory
Presenter:

Reducing the Cost of Persistence for Nonvolatile Heaps in End User Devices
Presenter:

The CloudSSD: Datacenter-Focused Design of Solid State Drives
Presenter:

Flash Physical Unclonable Function for Data Encryption
Presenter:

Adaptive parity distribution in parity-based RAID
Presenter:

Empirical FTL Evaluation and Modeling
Presenter:
Multi-Threaded Streamline Tracing on Data-Intensive Architectures
Presenter:

3D-integrated Storage Class Memory/NAND Flash Hybrid SSDs for Cloud Data Centers
Presenter:

Bounded Difference Constraints for PCM
Presenter:

ECC for Enterprise Flash Array on a Coarse Grained Programmable SoC
Presenter:

Block Device Interface for Unified Storage Memory
Presenter:

The Role of NVM in Low-Power SOC Design
Presenter: