Characterizing Flash Memory: Anomalies, Observations, and Applications

Laura M. Grupp*, Adrian M. Caulfield*, Joel Coburn*, Eitan Yaakobi†, Paul H. Siegel†, Jack K. Wolf†, Steven Swanson*

*Non-volatile Systems Laboratory, Department of Computer Science and Engineering
†Center for Magnetic Recording Research
Jacob’s School of Engineering
University of California, San Diego
Possible Applications

• Flash Translation Layers (FTLs)
• Operating System control
• Data encodings
• Heterogeneous SSD
• Data retention time
Test Setup

- Custom-Built Daughter Board
- Xilinx XUP Board
- Full-fledge Linux
- Kernel module

Erase
Read
Program
Repeat
10x Lifetime
# The Test Subjects

<table>
<thead>
<tr>
<th>Chip Name</th>
<th>Manufacturer</th>
<th>Tech Node</th>
<th>Capacity (Gb)</th>
<th>Page Size (B)</th>
<th>Pages/Block</th>
<th>Block/Plane</th>
<th>Planes/Die</th>
<th>Dies</th>
</tr>
</thead>
<tbody>
<tr>
<td>A-SLC2</td>
<td>A</td>
<td></td>
<td>2</td>
<td>2048</td>
<td>64</td>
<td>1024</td>
<td>2</td>
<td>1</td>
</tr>
<tr>
<td>A-SLC4</td>
<td>A</td>
<td></td>
<td>4</td>
<td>2048</td>
<td>64</td>
<td>4096</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>A-SLC8</td>
<td>A</td>
<td></td>
<td>8</td>
<td>2048</td>
<td>64</td>
<td>4096</td>
<td>2</td>
<td>1</td>
</tr>
<tr>
<td>B-SLC2</td>
<td>B</td>
<td>50nm</td>
<td>2</td>
<td>2048</td>
<td>64</td>
<td>2048</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>B-SLC4</td>
<td>B</td>
<td>72nm</td>
<td>4</td>
<td>2048</td>
<td>64</td>
<td>2048</td>
<td>2</td>
<td>1</td>
</tr>
<tr>
<td>E-SLC8</td>
<td>E</td>
<td></td>
<td>8</td>
<td>2048</td>
<td>64</td>
<td>4096</td>
<td>1</td>
<td>2</td>
</tr>
<tr>
<td>B-MLC8</td>
<td>B</td>
<td>72nm</td>
<td>8</td>
<td>2048</td>
<td>128</td>
<td>4096</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>B-MLC32</td>
<td>B</td>
<td>50nm</td>
<td>32</td>
<td>4096</td>
<td>128</td>
<td>2048</td>
<td>2</td>
<td>2</td>
</tr>
<tr>
<td>C-MLC64</td>
<td>C</td>
<td>43nm</td>
<td>64</td>
<td>8192</td>
<td>128</td>
<td>4096</td>
<td>1</td>
<td>2</td>
</tr>
<tr>
<td>D-MLC32</td>
<td>D</td>
<td></td>
<td>32</td>
<td>4096</td>
<td>128</td>
<td>4096</td>
<td>1</td>
<td>2</td>
</tr>
<tr>
<td>E-MLC8</td>
<td>E</td>
<td></td>
<td>8</td>
<td>4096</td>
<td>128</td>
<td>1024</td>
<td>1</td>
<td>2</td>
</tr>
</tbody>
</table>
The Tests
Quantify known and unknown properties

• Performance

• Energy Efficiency

• Reliability
The Tests

Quantify known complexities, look for new ones

• Performance

• Power & Energy

• Reliability
Program Latency Anomaly

- Fast 50% of Pages
- Slow 50% of Pages

Program Time (µs)

A-SLC2 A-SLC4 A-SLC8 B-SLC2 50nm B-SLC4 72nm E-SLC8 B-MLC8 72nm B-MLC32 50nm C-MLC64 43nm D-MLC32 E-MLC8

Page #:

0 1 2 3 4 5 6 7 8 9 ... 118 119 120 121 122 123 124 125 126 127
## High & Low Order Bits

<table>
<thead>
<tr>
<th>Flash State</th>
<th>Logical Data</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td><strong>High Order</strong></td>
</tr>
<tr>
<td></td>
<td>(fast)</td>
</tr>
<tr>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>1</td>
</tr>
</tbody>
</table>
Variation-Aware Interface

Extend Interface from MSR [Birrell et. al., 2005]

“High priority” == write to fast page

“Low priority” == write to any page

+ Lower latency when it matters
- Increase wear
Improving Paging Latency

- Paging in/out virtual memory == high priority
- Goal: reduce swap latency 40% faster
- Side effect: Increased Wear 3% increase

![Normalized Response Time Graph]

- Baseline Writes vs Swap Writes
- Time and Normalized Response
- Build, DeskDev, Financial, Average
MLC as SLC: Single Mode Level Cell?

Average cost per bit

<table>
<thead>
<tr>
<th></th>
<th>MLC: 31 ¢/Gbit</th>
<th>SLC: 94 ¢/Gbit</th>
</tr>
</thead>
</table>

MLC is 33% of SLC

DRAMeXchange
4/10/10
The Tests

Quantify known complexities, look for new ones

• Performance

• Power & Energy

• Reliability
From a representative datasheet →

**Peak Power**

<table>
<thead>
<tr>
<th>Operation</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sequential read</td>
<td>45</td>
<td>90</td>
<td>mW</td>
</tr>
<tr>
<td>Program</td>
<td>45</td>
<td>90</td>
<td>mW</td>
</tr>
<tr>
<td>Erase</td>
<td>45</td>
<td>90</td>
<td>mW</td>
</tr>
</tbody>
</table>
Energy: MLC

Program Energy (µJ)

- Fast Pages
- Slow Pages

B-MLC8 72nm
B-MLC32 50nm
C-MLC64 43nm
D-MLC32
E-MLC8
The Tests
Quantify known complexities, look for new ones

• Performance
• Energy Efficiency
• Reliability
SLC Wear Out

Lifetime

Program/Erase Cycles

Bit Error Rate

- A-SLC4
- B-SLC4 (72nm)
- A-SLC8
- E-SLC8
- B-SLC2 (50nm)
- A-SLC2

0.0E+00
1.0E-05
2.0E-05
3.0E-05
3.5E-05
0
50,000
100,000
150,000
200,000
250,000
300,000

0
50,000
100,000
150,000
200,000
250,000
300,000

5.0E-06
1.0E-05
1.5E-05
2.0E-05
2.5E-05
3.0E-05
3.5E-05
MLC Wear Out

Program/Erase Cycles

Bit Error Rate

D-MLC32
C-MLC64 (43nm)
B-MLC32 (50nm)
E-MLC8
B-MLC8 (72nm)

Lifetime
Read Disturb

The degradation of a bit by reading that cell or another.
Program Disturb

The degradation of a bit by **programming** that cell or another

Procedure:
Erase Block
Repeat:
  Program new data to one page
Program Disturb

![Graph showing Program Disturb for different memory technologies.

- E-SLC8
- B-MLC32 (50nm)
- C-MLC64 (43nm)
- D-MLC32
- E-MLC8

Y-axis: Bit Error Rate
X-axis: Number of Reprograms

Graph illustrates the bit error rate over the number of reprograms for various memory technologies, highlighting differences in performance and reliability.]
Program Disturb: 1 reprogram

• SLC: no errors for at least one reprogram

• MLC: errors for reprograms of certain pages
Write-Once Memory (WOM) Codes

Old Byte: 01110110
New Byte: 10000111

<table>
<thead>
<tr>
<th>Logical Bits</th>
<th>First Generation</th>
<th>Second Generation</th>
</tr>
</thead>
<tbody>
<tr>
<td>00</td>
<td>111</td>
<td>000</td>
</tr>
<tr>
<td>01</td>
<td>110</td>
<td>001</td>
</tr>
<tr>
<td>10</td>
<td>101</td>
<td>010</td>
</tr>
<tr>
<td>11</td>
<td>011</td>
<td>100</td>
</tr>
</tbody>
</table>

Program: 01 11 01 10
Reprogram: 10 00 01 11

<table>
<thead>
<tr>
<th>Physical</th>
<th>1st Gen.</th>
<th></th>
<th>2nd Gen.</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Physical</td>
<td>110</td>
<td>011</td>
<td>110</td>
</tr>
<tr>
<td>1st Gen.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Physical</td>
<td>010</td>
<td>000</td>
<td>110</td>
</tr>
<tr>
<td>2nd Gen.</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
WOM Codes and Flash

Procedure: Erase, Program, Reprogram, Repeat

**WOM-safe**: can be reprogrammed – use WOM encoding

**WOM-unsafe**: can’t be reprogrammed – don’t encode
Effective Lifetime

How many logical bits can we program per erase?

**SLC**

\[ 2 \times \frac{2}{3} \]

= 33% increase

**MLC**

\[ \frac{1}{2}(2 \times \frac{2}{3}) + \frac{1}{2}(1) \]

= 16.5% increase
WOM Codes – Lifetime Extension

Logical Bytes Written

<table>
<thead>
<tr>
<th></th>
<th>Baseline</th>
<th>WOM</th>
</tr>
</thead>
<tbody>
<tr>
<td>B-MLC8 72nm</td>
<td></td>
<td></td>
</tr>
<tr>
<td>B-MLC32 50nm</td>
<td></td>
<td></td>
</tr>
<tr>
<td>C-MLC64 43nm</td>
<td></td>
<td></td>
</tr>
<tr>
<td>D-MLC32</td>
<td></td>
<td></td>
</tr>
<tr>
<td>E-MLC8</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Up to: 5.2x increase

Up to: 5.2x increase
WOM Codes – Energy Reduction

Fewer erases per written bit

Average: 9% savings

Required Program Energy (nJ/bit)

Baseline WOM
Future Work

• Chips & Commands
  – more chips, higher densities
  – Other operations: cached, multi-plane

• Effects
  – Data retention
  – Data Dependence
  – Radiation Tolerance
  – Delay between Operations

• Applications
  – Error correction codes
  – Data encodings
  – New Applications
  – Interface Modifications
Conclusion

• Flash Memory beyond the datasheet
• Variation-Aware Interface:
  – Latency Reduction: average of 40%
  – Energy Savings: average of 13%
• Write Once Memory (WOM) Encoding
  – Lifetime Extension: up to 5.2x
  – Energy Savings: average of 9%
Thank You